

MIPI D-PHY IP User Guide

Agilex[™] 3 and Agilex[™] 5 FPGAs

Updated for Quartus® Prime Design Suite: **25.1**

IP Version: **5.0.0**



Online Version



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1. About the MIPI D-PHY IP

Altera offers native mobile industry processor interface (MIPI) D-PHY IP for Agilex™ 3 and Agilex 5 D-series and E-series devices.

Both Agilex 3 and Agilex 5 devices comply with MIPI D-PHY version 2.5, and allow transmission or reception of data with MIPI D-PHY interfaces. MIPI D-PHY provides the PHY-protocol interface (PPI) to connect with camera serial interface (CSI) and display serial interface (DSI) applications.

For more information about MIPI D-PHY performance and electrical requirement, refer to the Agilex 3 and Agilex 5 datasheets.

1.1. MIPI D-PHY IP Features

- Supports high-speed (HS) and low-power (LP) modes and allows direct interface with the D-PHY compliance component without external components.
- Performs up to 3.5 Gbps for D-Series and E-Series device group A and up to 2.5 Gbps for E-Series device group B and Agilex 3 devices for high-speed (HS) mode for data traffic
- Performs up to 20 MHz for low-power (LP) mode for control traffic.
- Each HSIO bank supports up to a maximum of 7 interfaces.
- Supports 1, 2, 4 or 8 data lanes per-interface, with one clock lane. The D-PHY lanes support only unidirectional operation.
- Includes an AXI-Lite interface for register access.

1.2. Unsupported Features

The following features are not supported in the MIPI D-PHY IP:

- Reverse Traffic
- HS-IDLE
- Half swing
- Alternate low-power (ALP)
- Bus turn around (BTA)
- Low-power contention detector (LP-CD)
- ALP-ED
- Spread-spectrum clock (SSC)
- 8B9B encoding

1.3. MIPI D-PHY IP Release Information

IP versions are the same as the Quartus® Prime Design Suite software versions up to v19.1. From Quartus Prime Design Suite software version 19.2 or later, IP cores have a new IP versioning scheme.

The IP version (X.Y.Z) number may change from one Quartus Prime software version to another. A change in:

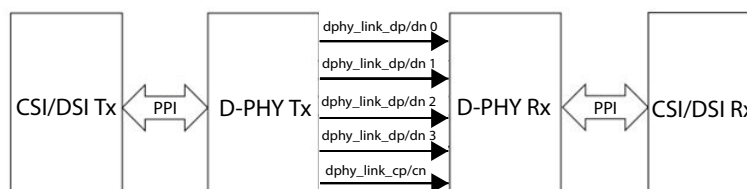
- X indicates a major revision of the IP. If you update your Quartus Prime software, you must regenerate the IP.
- Y indicates the IP includes new features. Regenerate your IP to include these new features.
- Z indicates the IP includes minor changes. Regenerate your IP to include these changes.

Table 1.

Item	Description
IP Version	5.0.0
Quartus Prime	25.1
Release Date	2025.03.31

1.4. MIPI D-PHY IP Block Diagram

Figure 1. MIPI D-PHY Block Diagram



1.5. Supported Data Lanes and Clock Lane Per Single HSIO Bank

Table 2. Interfaces per HSIO Bank

The table shows the number of supported interfaces for the HSIO bank based on the D-PHY lanes configuration. For a HSIO bank with less than 96 pins, the maximum interface reduces.

Mode	D-PHY Lanes	Maximum Interfaces per HSIO Bank
Transmitter (TX) or Receiver (RX)	1 data + 1 clock	7
	2 data + 1 clock	7
	4 data + 1 clock	7
	8 data + 1 clock	3

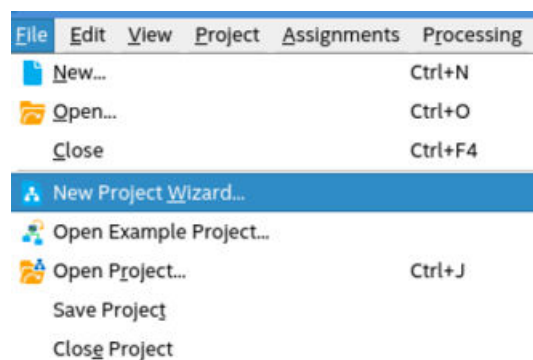
2. Configuring and Generating the MIPI D-PHY IP

This section describes how to generate the MIPI D-PHY IP using the IP Catalog in the Quartus Prime software, and explains the customizable parameters in the IP parameter editor.

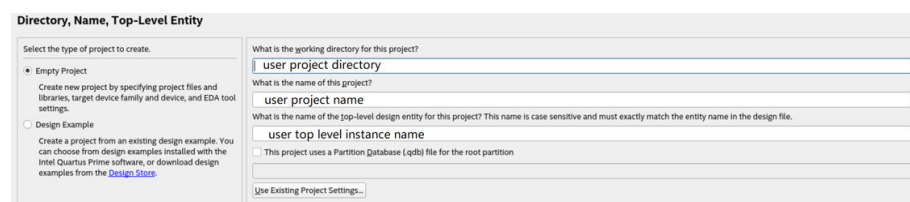
2.1. Creating a MIPI D-PHY Project

You must create a Quartus Prime project before generating the MIPI D-PHY IP and design example.

1. Launch the Quartus Prime software and select **File ► New Project Wizard** and click **Next**.



2. Specify a directory (*<user project directory>*), a name for the Quartus Prime project (*<user project name>*), and a top-level design entity name (*<user top-level instance name>*) that you want to create.
3. Verify that **Empty Project** is selected.



4. Under **Family**, select Agilex 3 or Agilex 5.
5. Under **Name filter**, type the device part number.
6. Under **Available devices**, select the appropriate device.

Family, Device & Board Settings

Device Board

Select the family and device you want to target for compilation. You can install additional device support with the Install Devices command on the Tools menu.

Device family

Family:

Device:

Show in 'Available devices' list

Package:

Pin count:

Core speed grade:

Target device

☒ Specific device selected in 'Available devices' list

☐ Other: n/a

☒ Show advanced devices

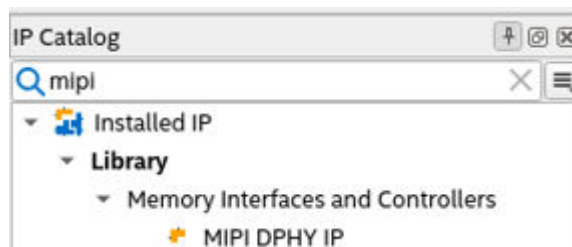
Filter:

	Name	Tile	Core Voltage	ALMs	Total I/Os	GPIOs	GT5 XCVR Channels	Memory Bits	M20K	DSP Blocks
1	A5EC0658B32AE5SR0		0.78V	222400	624	384	24	32993280	1611	846

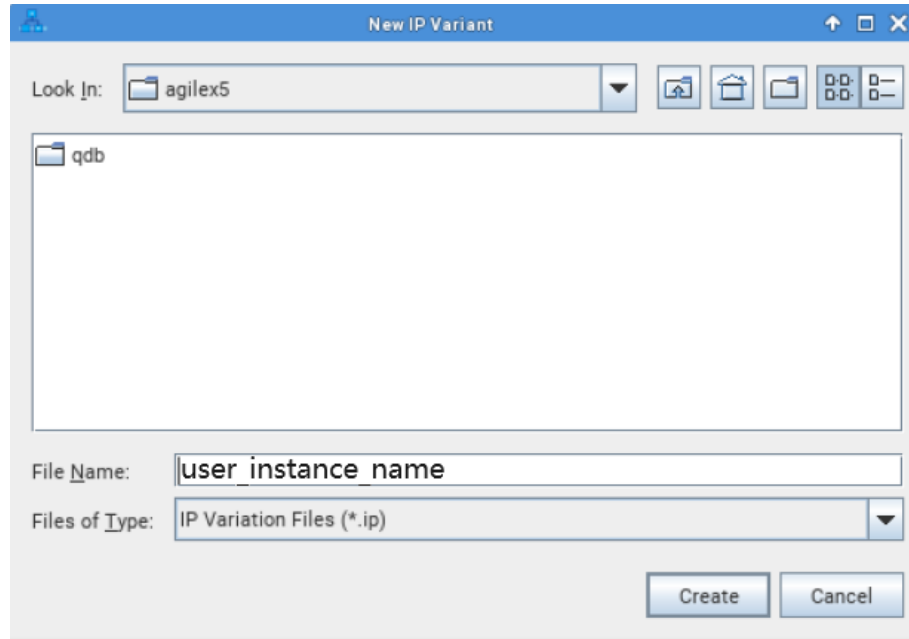
Available devices: 1

Help < Back Next > Finish Cancel

7. Click **Finish**.
8. In the **IP Catalog** window, select **MIPI DPHY IP**. (If the **IP Catalog** window is not visible, select **View > Utility Windows > IP Catalog** and double-click or click **+Add** for the IP parameter editor to appear.)



9. In the **IP Parameter Editor** provide an entity name for the MIPI DPHY IP (the name that you provide here becomes the file name for the IP) and specify a directory. Click **Create**.



10. The parameter editor has multiple tabs where you must configure parameters to reflect your MIPI D-PHY implementation.

The MIPI D-PHY IP Parameter Editor

The MIPI D-PHY IP parameter editor consists of a **D-PHY IP** tab and several **Link *n*** tabs.

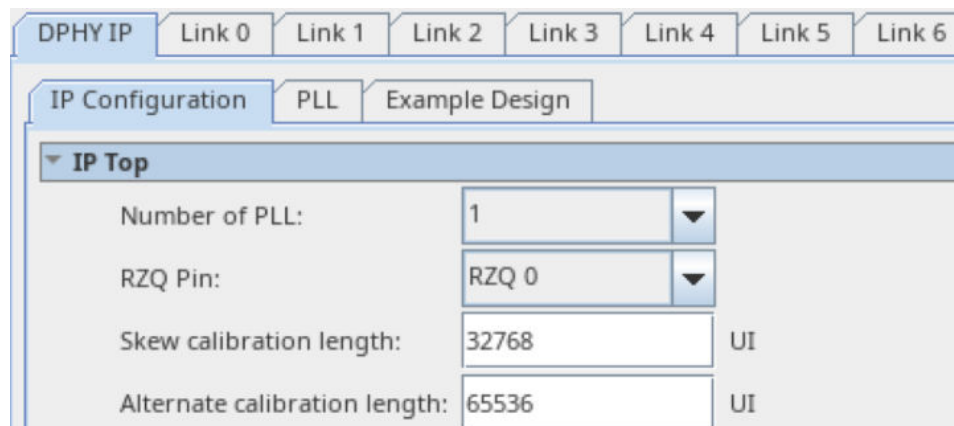
The **D-PHY IP** tab is where you configure general settings for the MIPI D-PHY IP instance. You specify the number of PLLs to use, the reference OCT calibration pin location, the skew calibration length, PLL settings, and design example generation settings.

The seven **Link *n*** tabs (numbered 0 through 6) correspond to the seven D-PHY interfaces, and are where you configure the channel link for each interface. Here, you can configure the byte location as D-PHY TX or D-PHY RX.

2.1.1. MIPI D-PHY IP Configuration Tab

This topic describes the configuration of the general settings on the D-PHY IP configuration tab in the parameter editor.

Figure 3. D-PHY IP Configuration Tab



The screenshot shows the 'D-PHY IP Configuration Tab' with the following settings:

- Number of PLL:** 1
- RZQ Pin:** RZQ 0
- Skew calibration length:** 32768 UI
- Alternate calibration length:** 65536 UI

Table 3. D-PHY IP Configuration Parameters

Parameter Name	Description	Setting
Number of PLL	Set number of PLL to use for clock generation. The IP can use up to 2 PLLs to share among the different D-PHY links. The bit rates of the D-PHY links has to be the same to share a PLL.	1 or 2. (Default value is 1.)
RZQ Pin	Set RZQ pin location to use for the D-PHY IP.	RZQ0 or RZQ1. (Default value is RZQ0.) Pin 38 in one I/O bank is RZQ0 and pin 62 is RZQ1. Pin 38 reserves BYTE LOCATION 3, and pin 62 reserves BYTE LOCATION 5.
Skew calibration length	Length of initial skew calibration pattern automatically generated by D-PHY TX IP when SKEW_CAL_EN = 1. This is done automatically after the t _{INIT} period. When SKEW_CAL_EN = 0, protocol IP is responsible to drive TxSkewCalHS to generate init skew sequence. SKEW_CAL_LEN is ignored by D-PHY RX IP.	32768 (This is the default value and the minimum.)
Alternate calibration length	Length of alternate calibration pattern automatically generated by D-PHY TX IP when ALT_CAL_EN = 1. This is done automatically after the init skew. When SKEW_CAL_EN = 0, protocol IP is responsible to drive TxAITCalHS to generate alt cal sequence. ALT_CAL_LEN is ignored by D-PHY RX IP.	65536 (This is the default value and the minimum.)

D-PHY IP PLL Tab

On the **PLL** tab, you configure the PLL settings such as core clock divider, PLL reference clock frequency, I/O standard selection, and V_{CO} clock frequency.

Figure 4. D-PHY IP PLL Tab

Table 4. D-PHY IP PLL Parameters

Parameter Name	Description	Setting
Core clock frequency divider	Set core clock frequency divider to generate core clock from VCO output. MIPI only supports divided by 4 or 8.	4 or 8. (Default value is 8.)
Reference clock frequency	PLL reference clock frequency.	10MHz - 300MHz. (Default value is 20MHz.)
Reference clock I/O type	Reference Clock I/O standard.	Single Ended 1.2V, LVDS 1.2V Single Ended 1.1V, LVDS 1.1V .
Share Reference Clock I/O	Enable PLL1 share reference clock with PLL0.	True or False. (Default value is True.)
VCO Clock Frequency	Sets the VCO clock frequency for PLL. - MIPI TX with bitrate > 1.2Gbps: VCO freq = 1/2 bit rate. - MIPI TX with bitrate 1.2Gbps: VCO freq = 1/2 bitrate * Tx bitrate divider (1, 2, 4 of 8). - MIPI RX with skew calibration disabled: no dependency between VCO freq and bit rate. -MIPI RX with skew calibration enabled: VCO freq = 1/2 bitrate	600MHz - 1740MHz.

2.1.2. MIPI D-PHY RX Mode

On the various **Link *n*** tabs, you can configure each channel link to act as a D-PHY transmitter (TX) or D-PHY receiver (RX). This topic discusses configuration for RX use.

You specify the MIPI D-PHY link location on the I/O bank during IP configuration. Look for the **Byte Location** parameter under the **Link *n* Location** for each *Link *n** tab. For the physical pin location of each byte location, refer to the table in the [Identifying Pin Assignments Based on Byte Location](#) topic.

Figure 5. Link Top Tab

The screenshot shows the 'Link Top' configuration tab for Link 0. The 'Link 0 Configuration' section includes the following settings:

- DPHY Role:** Rx
- Source PLL:** 0
- Bitrate:** 1600.0 Mbps
- PPI bus width:** 16 Bits
- Number of Lanes:** 1 Clk & 1 Data Lanes
- Continuous Clock:** False
- Free Running Clock Frequency:** 75.0 MHz

The 'Link 0 Location' section shows:

- Byte Location:** 0 within IO Bank

Table 5. Link Top Configuration Parameters

Parameter Name	Description	Setting
D-PHY Role	Configure D-PHY mode as Tx or Rx. If not using the channel, please remain it as unused.	TX/RX/Unused. (Default value is Unused.)
Source PLL	Specify which PLL source to drive the link's clock. 0 = PLL from Bottom Sub bank 1 = PLL from Top Sub bank	0 or 1. (Default value is 0.)
Bit Rate	Configure the MIPI D-PHY data rate.	Agilex 5 D-Series: 150 Mbps - 3,500 Mbps Agilex 5 E-Series device group A: 150 Mbps - 3,500 Mbps Agilex 5 E-Series device group B: 150 Mbps - 2,500 Mbps Agilex 3 C-Series: 150 Mbps to 2,500 Mbps
PPI bus width	Set PPI bus width for data lanes in the link : 16 bits.	16.
Number of Lanes	Set number of data lanes for the link : 1, 2, 4 or 8.	1 Data & 1 Clk 2 Data & 1 Clk 4 Data & 1 Clk 8 Data & 1 Clk (Default is 1 Data & 1 Clk.)

continued...

Parameter Name	Description	Setting
Continuous Clock	Specify that the clock lane is continuous.	True or False. (Default value is False.)
Free Running Clock Frequency	Rx free running clock frequency in MHz. When calibration is enabled, this will be fixed to RX clock.	
Byte Location	Specifies D-PHY links BYTE location within the I/O bank.	0-7.

Link Calibration Configuration

On the **Link Calibration** tab you can enable the skew and alternate calibration functions and RX equalization mode. You can run simulation to validate which RX equalization mode suits your design intent. For data rates at and above 2.0 Gbps with standard and long reference channel, you should set the **RX equalization mode** to *EQ SML*.

	<2.0 Gbps	≥2.0 Gbps
short	No	No
standard	No	Yes, CTLE small
long	No	Yes, CTLE small

Figure 6. Link Calibration Tab

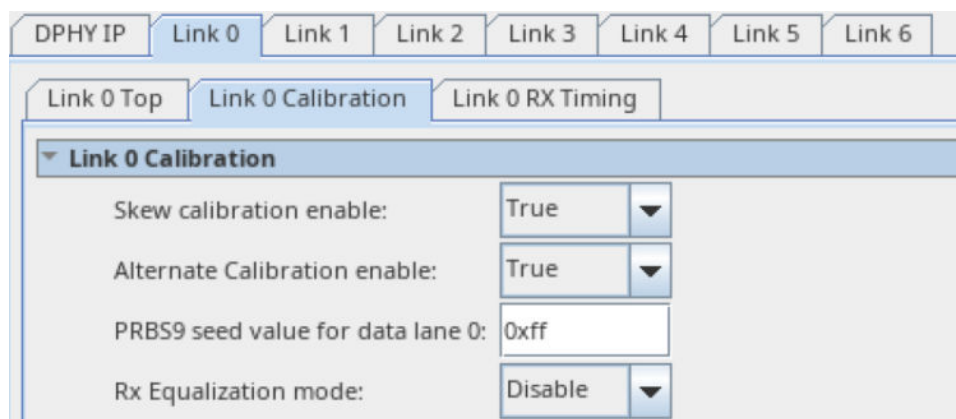


Table 6. Link Calibration Parameters

Parameter Name	Description	Setting
Skew Calibration Enable	Generate logic to support skew calibration.	True or False. (Default value is False.)
Alternate Calibration Enable	Generate logic to support alternate calibration. (Available when skew calibration mode is enabled.)	True or False. (Default value is False.)
PRBS9 seed value for data lane <i>n</i>	PRBS value for data lane used by Tx / Rx alt cal and test mode. (Available when Alternate Calibration is enabled.)	0xFF
Rx Equalization mode	Rx Equalization mode	Disable or EQ SML or EQ MED or EQ LRG . Default value is Disable .

Link RX Timing Configuration

On the **Link RX Timing** tab you can configure the receive timing parameters.

Figure 7. Link RX Timing Tab

The screenshot shows the 'Link 0 RX Timing' configuration window. It includes a 'Link 0 RX Timing Configuration' section with the following parameters:

- Timing Register Access Mode: RW
- Auto timing mode: Mid
- ☒ RX PCS Clock Loss Detect: 2 (FrClk, Approx = 106.67 ns)
- ☒ RX_CLK_SETTLE: 7 (FrClk, Approx = 193.33 ns)
- ☒ RX_HS_SETTLE: 1 (FrClk, Approx = 116.67 ns)
- ☒ RX_INIT: 12 (1024 x FrClk, Approx = 163840.00 ns)
- RX Data lane deskew delay 0: 0 (/64 UI)

Table 7. Link RX Timing Configuration Parameters

Parameter Name	Description	Setting
Timing Register Access Mode	Set to implement timing registers as R/W or RO. When using R/W mode, more register consumes in logic element resources.	RW or RO. (Default is RW.)
Auto Timing mode	Set Rx to be fixed at MID. Choose to use min timing, max timing or mid for default values of timing registers set to "Auto". All timing registers have a min specified timing, but not all have a max specified timing. For those with no max specified timing, max is set to register max value. <ul style="list-style-type: none"> Min – auto timing will set timing parameter to minimum required by specification (or 0 if below 0). Max – auto timing will set timing parameter to the maximum allowed by specification if such specification exists. If no maximum value is specified, auto timing will set it to 2x the minimum specification. Both values are set up to maximum allowable value based on register width. Mid – auto timing will set to (max + min) / 2. 	Max, Mid, or Min. (Default is Mid.)
RX PCS Clock Loss Detect	Timeout for D-PHY PCS to detect absence of Clock transitions and deassert RxClkActiveHS on the PPI bus. Min value should be equal to 3 x	0-255. (Default is 2.)

continued...

Parameter Name	Description	Setting
	RX_CLK-period (in ns). This is different from the D-PHY specification TCLK-MISS. This will be used to clock gate MIPI RX forwarded clock delay computations (approx): $- \text{TRX_CLK_LOSS_DETECT} = (\text{RX_CLK_LOSS_DETECT} + 6) * \text{Core_CLK_period}$.	
RX_CLK_SETTLE	Time interval during which the HS receiver should ignore any Clock Lane HS transitions, starting from the beginning of TCLK-PREPARE. Delay computation (approx): $\text{TRX-CLK-SETTLE} = (\text{RX_CLK_SETTLE} + 6) * \text{Core_CLK_period} + 2 * \text{RX_CLK_period}$.	0-255. (Default is 7.)
RX_HS_SETTLE	Time interval during which the HS receiver shall ignore any Data Lane HS transitions, starting from the beginning of THS-PREPARE. The HS receiver shall ignore any Data Lane transitions before the minimum value, and the HS receiver shall respond to any Data Lane transitions after the minimum val Delay computation (approx): $\text{THS-SETTLE} = (\text{RX_HS_SETTLE} + 7) * \text{Core_CLK_period} + \text{RX_CLK_period}$.	0-255. (Default is 1.)
RX_INIT	After power-up, the RX side PHY shall be initialized when the TX PHY drives a Stop State (LP-11) for a period longer than T_{INIT} . RX side shall ignore all Line states prior to this Initialization period.	0-255. (Default is 12.)
RX Data Lane deskew Delay 0	Manual data Lane 0 deskew delay setting .	0-63. (Default is 0.)

2.1.3. MIPI D-PHY TX Mode

On the various **Link *n*** tabs, you can configure each channel link to act as a D-PHY transmitter (TX) or D-PHY receiver (RX). This topic discusses configuration for TX use.

You specify the MIPI D-PHY link location on the I/O bank during IP configuration. Look for the **Byte Location** parameter under the **Link *n* Location** for each *Link *n** tab. For the physical pin location of each byte location, refer to the table in the [Identifying Pin Assignments Based on Byte Location](#) topic.

Figure 8. Link Top Tab

The screenshot displays the 'Link Top Tab' configuration window for Link 1. The 'Link 1 Configuration' section is expanded, showing various parameters for the DPHY role (Tx), PLL source (0), bitrate divider (1), and resulting bitrate (1200.0 Mbps). It also configures the PPI bus width (16 Bits), number of lanes (1 Clk & 1 Data), continuous clock (False), and free running clock frequency (75.0 MHz). The 'Link 1 Location' section indicates the byte location (1) within the IO Bank.

Table 8. Link Top Configuration Parameters

Parameter Name	Description	Setting
D-PHY Role	Configure D-PHY mode as Tx or Rx.	Unused, TX, or RX. (Default is Unused.)
Source PLL	Specify which PLL source will drive the link's clock.	0 or 1. (Default value is 0.)
Bit Rate Divider	Bit rate divider to keep VCO > 600MHz. Used to divide the TX bit rate.	1, 2, 4, or 8. (Default value is 8.)
Bit Rate	Not available for Tx mode.	Agilex 5 D-Series: 150 Mbps - 3,500 Mbps Agilex 5 E-Series device group A: 150 Mbps - 3,500 Mbps Agilex 5 E-Series device group B: 150 Mbps - 2,500 Mbps Agilex 3 C-Series: 150 Mbps - 2,500 Mbps
PPI bus width	Not available for Tx mode.	16.
Number of Lanes	Set number of data lanes for the link : 1, 2, 4 or 8.	1 Data & 1 Clk 2 Data & 1 Clk 4 Data & 1 Clk 8 Data & 1 Clk (Default is 1 Data & 1 Clk.)

continued...

Parameter Name	Description	Setting
Continuous clock	Specify that the clock lane is continuous.	True or False. (Default value is False.)
Free Running Clock Frequency	Not available for Tx mode.	
Byte location	Specifies D-PHY links BYTE location within the I/O bank.	0-7.

Link Calibration Configuration

On the **Link Calibration** tab you can enable the skew, alternate, and periodic calibration functions, preamble and TX equalization mode to meet your performance requirements. You can run simulation to validate which TX equalization mode suits your design intent. For data rates above 2.0 Gbps with standard and long reference channel, you should set the **TX equalization mode** to *MED LP* on Quartus Prime Pro Edition software version 24.2; if you are using version 24.1, select mode 1.

	≤2.0 Gbps	>2.0 Gbps
short	No	No
standard	No	Yes, Med LP
long	No	Yes, Med LP

Figure 9. Link Calibration Tab

The screenshot displays the 'Link 1 Calibration' configuration window. At the top, there are tabs for 'DPHY IP', 'Link 0', 'Link 1', 'Link 2', 'Link 3', 'Link 4', 'Link 5', and 'Link 6'. Below these, there are sub-tabs for 'Link 1 Top', 'Link 1 Calibration', and 'Link 1 TX Timing'. The 'Link 1 Calibration' sub-tab is selected, showing a list of calibration parameters with dropdown menus or text boxes for their values:

- Skew calibration enable: True
- Alternate Calibration enable: True
- Periodic calibration enable: False
- Preamble enable: True
- Preamble length: 32 UI
- PRBS9 seed value for data lane 0: 0xff
- Tx Equalization mode: Disable

Table 9. Link Calibration Parameters

Parameter Name	Description	Setting
Skew Calibration Enable	Generate logic to support skew calibration.	True or False. (Default value is False.)
Alternate Calibration Enable	Generate logic to support alternate calibration (Show when skew calibration enabled).	True or False. (Default value is False.)
Periodic calibration enable	Generate logic to support periodic skew calibration (Show when skew calibration enabled).	True or False. (Default value is False.)
Preamble Enabled	Generate logic to support preamble.	True or False. (Default value is False.)
Preamble Length	Preamble length settings (when Preamble is enabled).	32,64,96,128,160,192,224,256,288,320,352,384,416,448,480,512 UI. (Default value is 32.)
PRBS9 seed value for data lane n	PRBS value for data lane used by Tx / Rx alt cal and test mode. (Available when Alternate Calibration is enabled.)	0xFF
Tx equalization mode	Tx Equalization mode.	Disable or MED LP or HI LP or MED CZ. (Default value is Disable.)

Link TX Timing Parameters

On the **Link TX Timing** tab you can configure the transmit timing parameters..

Figure 10. Link TX Timing Tab

Link 1 TX Timing Configuration

Timing Register Access Mode: RW

Auto timing mode: Mid

Tx Clock Phase Shift: 32 /64 UI

Parameter	Value	Unit	Approx. Value
<input checked="" type="checkbox"/> TX_LPX:	6	FrClk	Approx = 80.00 ns
<input checked="" type="checkbox"/> TX_HS_EXIT:	12	FrClk	Approx = 160.00 ns
<input checked="" type="checkbox"/> TX_LP_EXIT:	12	FrClk	Approx = 160.00 ns
<input checked="" type="checkbox"/> TX_CLK_PREPARE:	2	FrClk	Approx = 53.33 ns
<input checked="" type="checkbox"/> TX_CLK_TRAIL:	7	FrClk	Approx = 80.00 ns
<input checked="" type="checkbox"/> TX_CLK_ZERO:	22	FrClk	Approx = 360.00 ns
<input checked="" type="checkbox"/> TX_CLK_POST:	3	FrClk	Approx = 120.00 ns
<input checked="" type="checkbox"/> TX_CLK_PRE:	3	FrClk	Approx = 26.67 ns
<input checked="" type="checkbox"/> TX_HS_PREPARE:	3	FrClk	Approx = 66.67 ns
<input checked="" type="checkbox"/> TX_HS_ZERO:	4	FrClk	Approx = 133.33 ns
<input checked="" type="checkbox"/> TX_HS_TRAIL:	8	FrClk	Approx = 80.00 ns
<input checked="" type="checkbox"/> TX_INIT:	12	1204 x FrClk	Approx = 163840.00 ns
<input checked="" type="checkbox"/> D-PHY TX tWAKE:	111	1024 x FrClk	Approx = 1515520.00 ns

* UI = 0.833 ns; FrClk period (Core_CLK_period) = 13.33 ns

Table 10. Link TX Timing Parameters

Parameter Name	Description	Setting
Timing Register Access Mode	Set to implement timing registers as R/W or RO. R/W register will use up more FPGA resources.	RW or RO. (Default value is RW.)
Auto Timing mode	Choose to use min timing, max timing or mid for default values of timing registers set to "Auto". All timing registers have a min specified timing, but not all have a max specified timing. For those with no max specified timing, max Is set to register max value.	Max or Mid or Min. (Default value is Mid.)
TX Clock Phase Shift	Sets the phase shift of the clock lane relative to the data lanes. 1 UI is equivalent to 64 steps. Default is 32, shifting clock by 1/2 UI.	0-63. (Default value is 32.)

continued...

Parameter Name	Description	Setting
TX_LPX	Transmitted length of any Low-Power state period. TLPX is an internal PHY timing parameter. TCLK-PREPARE is an external parameter, which can differ from TLPX.	0-128. (Default value is 6.)
TX_HS_Exit	Time that the transmitter drives LP-11 following a HS burst.	0-255. (Default value is 12.)
TX_LP_Exit	Time that the transmitter drives LP-11 between any LP sequences, or between an LP sequence and a HS burst.	0-255. (Default value is 12.)
Tx_CLK_Prepere	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission. Delay computation (approx): $TCLK_PREPARE = (TX_CLK_PREPARE + 2) * Core_CLK_period$.	0-63. (Default value is 2.)
Tx_Clk_Trail	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst. Delay computation (approx): $TCLK_TRAIL = (TX_CLK_TRAIL - TXFIFO_LAT) * Core_CLK_period$ where TXFIFO_LAT might be different for PPI = 16 and 8.	0-127. (Default value is 7.)
Tx_clk_zero	Time that the transmitter drives the HS-0 state prior to starting the Clock. Delay computation (approx): $(+ TXFIFO_LAT \text{ is intended}) TCLK_ZERO = (TX_CLK_ZERO + 2 + TXFIFO_LAT) * Core_CLK_period$.	0-127. (Default value is 22.)
Tx_clk_Post	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP mode. Interval is defined as the period from the end of THS-TRAIL to the beginning of TCLK-TRAIL. Delay computation (approx) : $(+ TXFIFO_LAT \text{ is intended}) TCLK_POST = (TX_CLK_POST + 2 + TXFIFO_LAT - (2 * TX_VCO_FREQ_MULT)) * Core_CLK_period$. TX_VCO_FREQ_MULT is the Bit Rate Divider value described on table 14 to target Low Bit Rate speeds on our RX IP.	0-255. (Default value is 3.)
Tx_CLK_Pre	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode. Delay computation: $TCLK_PRE = (TX_CLK_PRE + 2 - TXFIFO_LAT) * Core_CLK_period$ Aligned to data lanes' next ESC clock edge.	0-15. (Default value is 3.)
Tx_HS_Prepere	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission. Delay computation (approx): $THS_PREPARE = (TX_HS_PREPARE + 2) * Core_CLK_period$.	0-63. (Default value is 3.)
continued...		

Parameter Name	Description	Setting
Tx_HS_Zero	Time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence. Delay computation (approx): $(+ \text{TXFIFO_LAT is intended})$ $\text{THS-ZERO} = (\text{TX_HS_ZERO} + 4 + \text{TXFIFO_LAT}) * \text{Core_CLK_period}.$	0-255. (Default value is 4.)
Tx_HS_Trail	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst. Delay computation (approx): $\text{THS-TRAIL} = (\text{TX_HS_TRAIL} + 1 - \text{TXFIFO_LAT} - (\text{TX_VCO_FREQ_MULT} > 2 ? 8 : 2)) * \text{CORE_CLK_period}.$ TX_VCO_FREQ_MULT is the Bit Rate Divider value described on table 14 to target Low Bit Rate speeds on our RX IP.	0-255. (Default value is 8.)
Tx_Init	Time that Slave side PHY shall be initialized when the Master PHY drives a Stop State.	0-255. (Default value is 12.)
D-PHY Tx Twake	Time that a transmitter drives a Mark-1 state prior to a Stop state in order to initiate an exit from ULPS.	0-255. (Default value is 111.)

2.2. Generating the Design Example

An automated design example flow is available for the MIPI D-PHY IP.

You can generate a design example that matches the MIPI D-PHY IP that you require. You can use the design example to assist your evaluation, or as a starting point for your own system. For successful design example generation, you must enable at least one link by selecting for TX or RX implementation.

1. Click **Example Design** tab and specify your parameters.

Figure 11. Example Design Tab

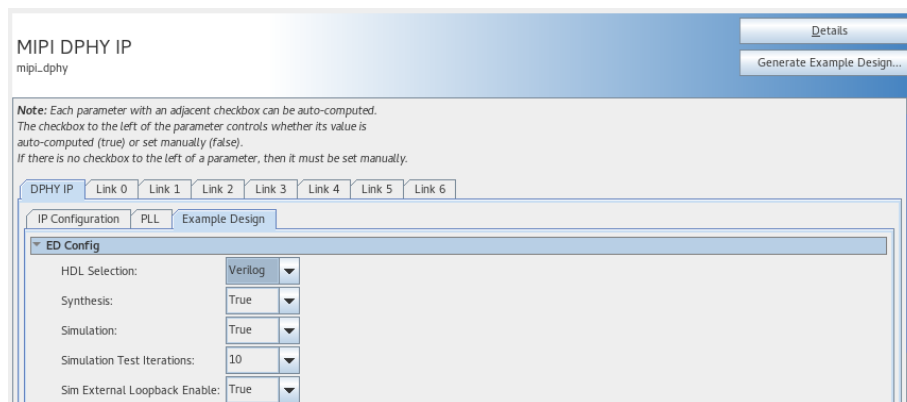


Table 11. Example Design Parameters

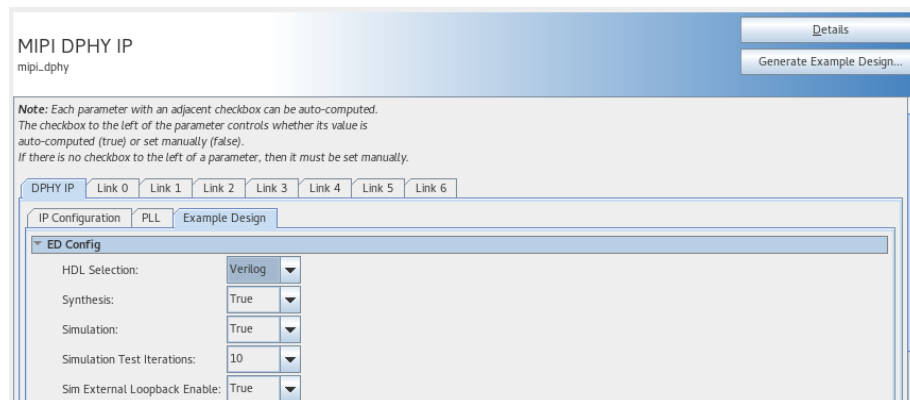
Parameter	Setting	Description
HDL Selection	Verilog HDL or VHDL (default value is Verilog HDL).	Hardware description language (HDL) selection.
Synthesis	True or False. (Default value is True.)	Generate synthesis design example, which consists of: <ul style="list-style-type: none"> D-PHY IP PPI traffic generator; 1 for each TX link. PPI pattern checker; 1 for each RX link. JTAG bridge to access CSR registers. Reset release IP. Interconnect blocks.
Simulation	True or False. (Default value is True.)	Generate simulation design example.
Simulation Test Iterations	1-1023. (Default value is 10.)	Number of test iteration.
Sim External Loopback Enabled	True or False. (Default value is True.)	Generation simulation design example with external loopback.

- Click **Generate Example Designs** to specify and generate the synthesis and simulation design example file sets that you can use to validate your MIPI D-PHY IP.

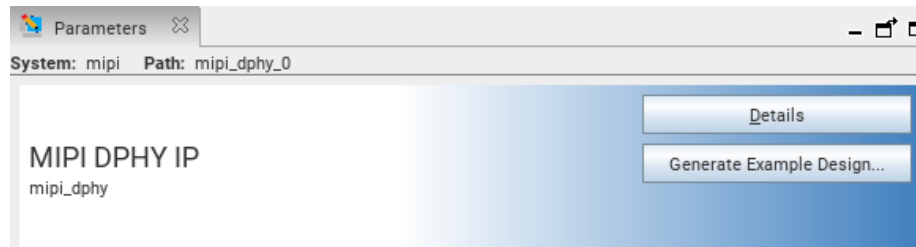
2.2.1. Generating the Synthesizable MIPI D-PHY Design Example

To generate the synthesizable design example, follow the steps below.

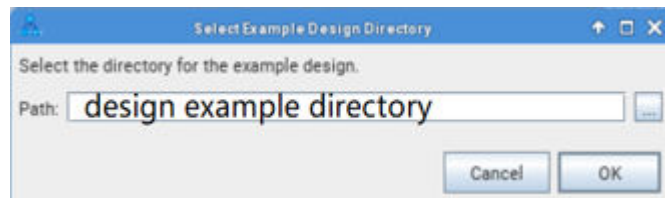
- On the **Example Design** tab, ensure that the **Synthesis** box is set as **True**.



- Configure the parameters as appropriate for your needs and click **File ► Save** to save the current settings into the IP variation file (*<user instance name>.ip*).
- Click **Generate Example Design** in the upper-right corner of the window.



4. Specify a directory for the MIPI D-PHY design example and click **OK**. Successful generation of the design example creates the synthesis file set under a *qii* directory.



5. Click **File > Exit** to exit the **IP Parameter Editor Pro** window. The system prompts: Recent changes have not been generated. Generate now?. Click **No** to continue with the next flow.
6. To open the design example, click **File > Open Project**, navigate to `<project_directory>/<design_example_name>/qii/ed_synth.qpf`, and click **Open**.

2.2.1.1. Design Example Block Diagram

The MIPI DPHY synthesis design example contains the major blocks shown in the figure below.

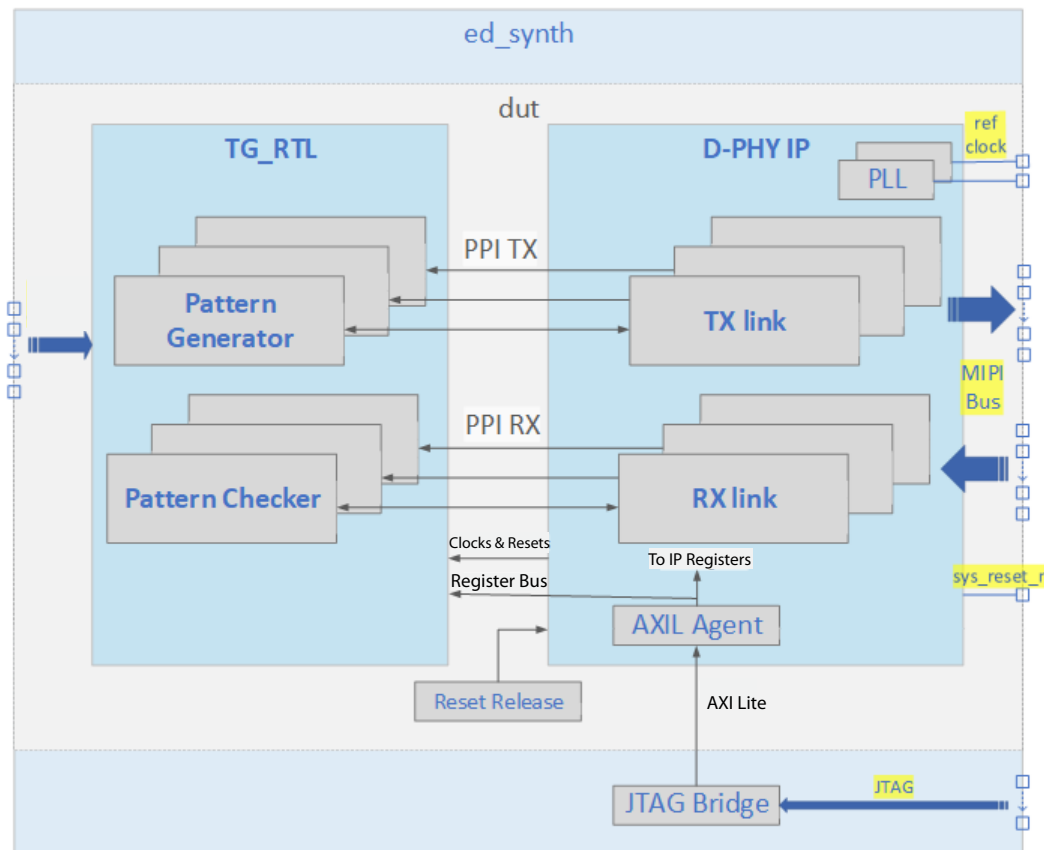
Pattern checker: The traffic generator pattern checker monitors D-PHY RX PPI bus activities and compares with the expected behavior. The expected activities mirror the pattern generator's activity including the expected data and number of iterations.

The pattern generator generates both *fail* and *done* signals. The *fail* signal is asserted immediately after an error condition is detected and stays asserted until the test is restarted. The *done* signal is asserted when all the enabled tests have reached the expected number of iterations.

Pattern generator: The role of the pattern generator is to create PPI traffic, both HS and LP.

D-PHY IP: The D-PHY IP provides the physical layer implementation of the MIPI D-PHY interface. The PHY converts the parallel PPI bus to/from the serial MIPI D-PHY interface.

Figure 12. Design Example Top-Level Diagram for Synthesis



2.2.1.2. External Interfaces

The following table lists the external interfaces available to the design example.

Table 12. Design Example Interfaces

Signal	Direction	Width	Description
Global Signals			
sys_rst_reset_n	Input	1	System asynchronous reset.
ref_clk_0_clk	Input	1	Reference clock input for PLL 0. Ref_clk_0_n is only necessary if using LVDS reference clock input.
ref_clk_0_clk_n			
ref_clk_1_clk	Input	1	Reference clock input for PLL 1 when used. Ref_clk_1_n is only necessary if using LVDS reference clock input.
ref_clk_1_clk_n			
rzq_rzq	Input	1	RZQ pin used for ODT calibration.
MIPI Interface (1 per link <i>n</i>)			
LINK _{<i>n</i>} _D-PHY_link_cp	TX – Output RX – Input	1	D-PHY clock lane pins for link <i>n</i> .
<i>continued...</i>			

Signal	Direction	Width	Description
LINK n _D-PHY_link_cn			
LINK n _D-PHY_link_dp	TX – Output RX – Input	m	D-PHY data lane pins for link n (where n is the number of data lanes = 1,2,4 or 8).
LINK n _D-PHY_link_dn			

2.3. Compiling the Design Example

1. Navigate to the Quartus Prime directory containing the design example directory
2. Open the Quartus Prime project file, (.qpf).
3. Click **Processing ► Start Compilation**. After a successful compilation, the software generates a .sof file, which enables the design to run on hardware

3. MIPI D-PHY Interface Design Guidelines

This section provides the board design guidelines that you must observe when implementing your MIPI D-PHY design on a circuit board.

Note: For information on MIPI interface layout design guidelines, refer to the document *High-Speed Signal Printed Circuit Board (PCB) Design Guidelines (HSSI, EMIF, MIPI, LVDS, PDN)*.

3.1. Identifying Pin Assignments Based on Byte Location

In the MIPI D-PHY GUI, you must provide the pin placement location via the byte location. Look for the **Byte Location** parameter under the **Link *n* Location** for each **Link *n*** tab. Refer to the pin index table below for each MIPI configuration on the I/O bank. You can refer to the device pin-out files to identify the pin location with reference to the pin index. You can assign the pin location with the pin location identified.

Example for MIPI D-PHY design using 2 data lanes and 1 clock lane assigned to byte location 7: The pin index 84 and 85 are for data lane 0 (D0), pin index 86 and 87 are for data lane 1 (D1), and pin index 88 and 89 are for the clock lane (CLK).

Example for MIPI D-PHY design using 2 data lanes and 1 clock lane assigned to byte location 6: The pin index 72 and 73 are for data lane 0 (D0), pin index 74 and 75 are for data lane 1 (D1), and pin index 76 and 77 are for the clock lane (CLK).

Table 14. MIPI Pin Assignments Based on Byte Location

Pin Index *	Byte Location	Number of MIPI Lanes			
		x1	x2	x4	x8
95	7				
94					
93				D3	D7
92					
91***				D2	D6
90					
89					
88		CLK	CLK	CLK	
87			D1	D1	D5
86					
85		D0	D0	D0	D4
continued...					

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*Other names and brands may be claimed as the property of others.

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Pin Index *	Byte Location	Number of MIPI Lanes			
		x1	x2	x4	x8
84					
83	6				
82					
81				D3	D3
80				D2	D2
79***				D2	D2
78				D2	D2
77				D2	D2
76		CLK	CLK	CLK	CLK
75				D1	D1
74			D1	D1	D1
73			D0	D0	D0
72		D0	D0	D0	
71	5				
70					
69				D3	D7
68				D3	D7
67***				D2	D6
66				D2	D6
65				D2	D6
64		CLK	CLK	CLK	
63				D1	D5
62**			D1	D1	D5
61			D0	D0	D4
60		D0	D0	D4	
59	4				
58					
57				D3	D3
56				D3	D3
55***				D2	D2
54				D2	D2
53				D2	D2
52		CLK	CLK	CLK	CLK
51				D1	D1
50			D1	D1	D1
continued...					

Pin Index *	Byte Location	Number of MIPI Lanes			
		x1	x2	x4	x8
49		D0	D0	D0	D0
48					
47	3				
46					
45				D3	D7
44					
43***				D2	D6
42					
41		CLK	CLK	CLK	
40					
39			D1	D1	D5
38**					
37		D0	D0	D0	D4
36					
35	2				
34					
33				D3	D3
32					
31***				D2	D2
30					
29		CLK	CLK	CLK	CLK
28					
27			D1	D1	D1
26					
25		D0	D0	D0	D0
24					
23	1				
22					
21				D3	D7
20					
19***				D2	D6
18					
17		CLK	CLK	CLK	
16					
15			D1	D1	D5

continued...

Pin Index *	Byte Location	Number of MIPI Lanes			
		x1	x2	x4	x8
14	0				
13					
12		D0	D0	D0	D4
11	0				
10					
9				D3	D3
8					
7***				D2	D2
6					
5		CLK	CLK	CLK	CLK
4					
3			D1	D1	D1
2					
1					
0		D0	D0	D0	D0

Note: * Based on the pin index, the even number is P pin and odd number is N pin for data lane or clock lane.
 ** These pins can be use as RZQ pin. Refer to [Assigning RZQ Pin and Dedicated Reference Clock Pin for MIPI D-PHY IP](#) for more details.
 *** Unused Pin 7 on the same I/O byte location for design with 1 or 2 data lanes plus 1 clock, should be left unused. Refer to [Using the Remaining I/O Pin from Same Byte Location](#) for details.

3.2. Assigning the RZQ pin and Dedicated Reference Clock Pin for MIPI D-PHY IP

The MIPI D-PHY IP must use the dedicated RZQ pin for OCT calibration.

The RZQ pin must be placed at byte location 3 (at pin index 38) or byte location 5 (at pin index 62). You can select the RZQ pin location during IP generation. Look for the **RZQ Pin** parameter on the **IP Configuration** tab under the **DPHY IP** tab. Selecting *RZQ 0* places the RZQ pin in byte location 3, while selecting *RZQ 1* places the RZQ pin in byte location 5.

When an RZQ pin is used, you cannot use the remaining pin from the same BYTE location for MIPI D-PHY functions. For example, when placing the RZQ pin at pin index 62, you cannot use the remaining I/O pin on byte location 5 for the MIPI D-PHY IP. The RZQ pin must connect to a 240Ω onboard resistor. You cannot share the RZQ pin used for the MIPI D-PHY IP with an EMIF IP from the same I/O bank.

You must assign the MIPI D-PHY IP reference clock pin to a dedicated reference clock pin. To optimize the pin assignment, you can place the MIPI D-PHY IP reference clock pin and RZQ pin from the same byte location. For example, for an RZQ pin at index 62, you can use the dedicated clock pins at pin index locations 61 and 60 for the reference clock pins for MIPI D-PHY IP.

You can configure the reference clock pin I/O standard as LVCMOS or true differential signaling at the same VCCIO_PIO level. The I/O standard assignment is available in the MIPI D-PHY IP GUI. For a reference clock with a true differential signaling I/O standard, you cannot use the remaining pin from the same BYTE location for MIPI D-PHY functions. You can place the reference clock pins in the same byte location as the RZQ pin. For a reference clock with an LVCMOS I/O standard, you can use the remaining pin from the same BYTE location for MIPI D-PHY functions.

3.3. Rules for the Remaining I/O Pin from Same Byte Location

The following rules apply for the remaining I/O pins from the same byte location occupied by MIPI D-PHY:

The MIPI D-PHY with 1 data plus 1 clock have pins 2, 3, and 6 to 11 on the same byte location, unoccupied. The MIPI D-PHY with 2 data plus 1 clock have pins 6 to 11 on the same byte location, unoccupied. For a design with 1 or 2 data lanes plus 1 clock, pin 7 (pin index 7 or 19 or 31 or 43 or 55 or 67 or 79 or 91) on the same byte location should be left unused. This rule does not apply to designs with 4 or 8 data lanes plus 1 clock, because pins 7 and 8 serve as MIPI D-PHY data lane.

You can use the remaining I/O pins only for LVCMOS1.1 or LVCMOS1.2 for general function, or SLVS-400 with or without LVDS SERDES function. The remaining I/O pins cannot be used for other functions.

3.4. I/O Bank Sharing

You can use the remaining unused I/O lanes in the I/O bank for MIPI with other implementations using the same I/O voltage.

The MIPI D-PHY IP currently supports 1.1 V or 1.2 V implementation. The MIPI D-PHY pin uses the D-PHY I/O standard in the Quartus Prime software.

The MIPI D-PHY IP allows reference clock I/O type selection of 1.1V or 1.2V voltage level with differential or single-ended I/O standards. The MIPI D-PHY IP defaults the VCCIO_PIO on each pin based on the reference clock voltage level. This is done through the .QIP file that is generated with the MIPI D-PHY design. The default reference clock I/O type setting for MIPI D-PHY IP is single-ended 1.2V. This sets all the corresponding pins in the MIPI D-PHY design to 1.2V. If you are targeting 1.1V, set the reference clock I/O type to 1.1V differential or single-ended I/O standard.

For MIPI D-PHY using the Quartus Prime software version 24.3 or earlier, the VCCIO_PIO of the sub-bank defaults to 1.2V when the D-PHY I/O standard is used.

Follow these steps if you are using the Quartus Prime software 24.3 or earlier and intend to use D-PHY at 1.1V VCCIO_PIO:

1. Assign the MIPI D-PHY reference clock and RZQ pin to 1.1 V with a QSF assignment or in the Pin Planner. The reference clock can be LVCOMS or true differential signaling, depending on the selection on the MIPI D-PHY IP.
2. Use the following QSF assignment to assign the VCCIO_PIO of the sub-bank to 1.1 V. You must set the assignment for both top and bottom sub-bank if your MIPI D-PHY design is placed on both the top and bottom sub-banks:

```
set_global_assignment -name IOBANK_VCCIO 1.1V -section_id <sub_bank_name>
```

For example:

```
set_global_assignment -name IOBANK_VCCIO 1.1V -section_id 3B_B
```

3.5. MIPI D-PHY Placement Rules

When implementing a MIPI D-PHY design, you must follow the placement rules. Some I/O pins cannot be implemented as single-ended pins.

Example: For a MIPI D-PHY design with 4 data lanes and 1 clock lane on byte location 1, the I/O pin with pin index 5, 10, 23 and 26 cannot be implemented as single ended pins

For general purpose I/O placement guidelines, follow the I/O placement restrictions in the *Agilex 5 General-Purpose I/O User Guide*.

Table 15. MIPI D-PHY Lanes and Restricted Pin Locations

Byte Location	MIPI D-PHY Lanes	Restricted Pin Location
Byte location 0	1 data + 1 clock	Pin index 3 and 15.
	2 data + 1 clock	Pin index 15. Pin index 88 from adjacent bank. ⁽¹⁾
	4 data + 1 clock	Pin index 11 and 15. Pin index 88 and 95 from adjacent bank. ⁽¹⁾
Byte location 1	1 data + 1 clock	Pin index 14 and 26.
	2 data + 1 clock	Pin index 5 and 26.
	4 data + 1 clock	Pin index 5, 10, 23 and 26.
Byte location 0 and 1	8 data + 1 clock	Pin index 10, 11, 17 and 23. Pin index 88 and 95 from adjacent bank. ⁽¹⁾
Byte location 2	1 data + 1 clock	Pin index 27 and 39.
	2 data + 1 clock	Pin index 16 and 39.
	4 data + 1 clock	Pin index 16, 22, 34 and 39.
Byte location 3	1 data + 1 clock	Pin index 38 and 50.
	2 data + 1 clock	Pin index 29 and 50.
	4 data + 1 clock	Pin index 29, 35, 47 and 50.
Byte location 2 and 3	8 data + 1 clock	Pin index 16, 22, 34, 35, 41 and 47.
Byte location 4	1 data + 1 clock	Pin index 51 and 63.
	2 data + 1 clock	Pin index 40 and 63.
	4 data + 1 clock	Pin index 40, 46, 58 and 63.
Byte location 5	1 data + 1 clock	Pin index 62 and 74.
	2 data + 1 clock	Pin index 53 and 74.
	4 data + 1 clock	Pin index 53, 59, 71 and 74.
Byte location 4 and 5	8 data + 1 clock	Pin index 40, 46, 58, 59, 65 and 71.
continued...		

⁽¹⁾ The adjacent pins do not apply to Agilex 3 C-Series devices.

Byte Location	MIPI D-PHY Lanes	Restricted Pin Location
Byte location 6	1 data + 1 clock	Pin index 75 and 87.
	2 data + 1 clock	Pin index 64 and 87.
	4 data + 1 clock	Pin index 64, 70, 82 and 87.
Byte location 7	1 data + 1 clock	Pin index 86. Pin index 2 from adjacent bank. ⁽¹⁾
	2 data + 1 clock	Pin index 77. Pin index 2 from adjacent bank. ⁽¹⁾
	4 data + 1 clock	Pin index 77, 83 and 94. Pin index 2 from adjacent bank. ⁽¹⁾
Byte location 6 and 7	8 data + 1 clock	Pin index 64, 70, 82, 83, 89 and 94.

3.6. Handling MIPI D-PHY IP Reset

You must use the reset-release IP to hold the MIPI D-DPHY IP reset (arst_n) in reset until the device has fully entered user mode.



4. Simulating the MIPI D-PHY IP

To simulate your design you require the following components:

- A simulator. The simulator must be an Altera-supported Verilog HDL simulator:
 - Siemens EDA ModelSim
 - Synopsys VCS/VCS-MX
- A design using the MIPI D-PHY IP with external loopback enabled
- An example driver or traffic generator (to initiate read and write transactions)
- A testbench and a suitable memory simulation model

4.1. Simulating the MIPI D-PHY IP Design Example with External Loopback Enabled

The MIPI D-PHY IP allows you to generate the design example with external loopback that includes the MIPI D-PHY IP and traffic generator. Run this design example to validate your MIPI IP operation.

1. On the **Example Design** tab, set the **Simulation** parameter to **True**.
2. On the **Example Design** tab under the **D-PHY IP** tab, ensure that the **Sim External Loopback Enable** parameter is set to true.
3. For both the RX and TX link, ensure that that you enable the calibration settings according to the requirement of the operating data rate. .
4. Ensure that both the RX and TX links have the same bit rate and number of data lanes.
5. Configure the parameters as appropriate for your needs and click **File ► Save** to save the current settings into the IP variation file (`<user instance name>.ip`)

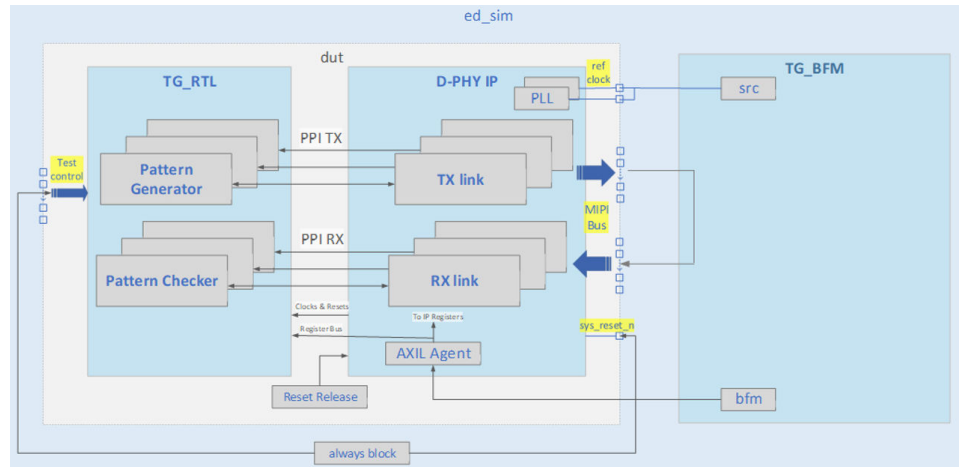
4.1.1. Simulation Design Example with External Loopback Enabled Block Diagram

The MIPI D-PHY IP supports a loopback-enabled option. In the example below, a single D-PHY IP has both the matching TX and RX links instantiated within the same IP.

Alternatively, you could instantiate two IPs for TX and RX, respectively. When TX and RX links are instantiated within the same IP, the D-PHY IP checks for the RX-TX pairing for loopback and passes that information to the TG_BFM block for enabling the loopbacks among the different links.

The simulation design example with external loopback enabled contains the major blocks shown in the figure below:

Figure 13. External Loopback Simulation Testbench



As described in the previous section, the synthesis design example contains a traffic generator and an instance of the D-PHY IP.

The TG_BFM model, which includes the following functions:

- Clock source for PLL reference clock.
- AXI-Lite interface instantiation which contains read/write tasks and can be used as an AXI-Lite BFM.
- Loopback MUXing for looping back TX links to RX links on the same D-PHY IP.

4.1.2. Simulating MIPI D-PHY IP Design Example with Modelsim* and Questasim*

1. At the command prompt, change the working directory:
`<example_design_directory>/sim/ed_sim/mentor`
2. Invoke vsim by typing `vsim`, which launches a window where you can run the following commands.
3. Execute the following command in the transcript terminal:

```
source msim_setup.tcl
```

4. Run the following command in the transcript terminal:

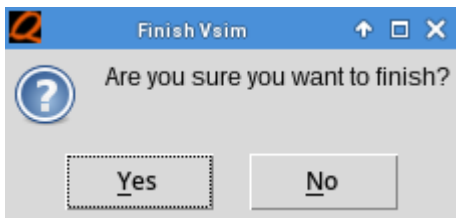
```
ld_debug
```

5. After the command completes, you can add the desired signal to observe by right clicking and selecting **Add Wave**.

6. To perform the simulation, run the following command:

```
run -all
```

7. When the simulation has completed, a dialog box appears, asking if you want to finish. Click **No**, return to the simulator, and analyze the waveform that you have added.



8. A successful simulation displays the following message:

```
Simulation completed successfully (SIMULATION PASSED).
```

4.1.3. Simulating MIPI D-PHY IP Design Example with Synopsys VCSMX* and Xcelium*

The following example illustrates the VCSMX simulator; follow similar steps for the other simulators.

1. Navigate to the working directory: `<example_design_directory>/sim/ed_sim/synopsys/vcsmx`
2. To run a simulation in non-interactive mode, type the following command in a single line:

```
sh vcsmx_setup.sh
```

3. A successful simulation displays the following message:

```
Simulation completed successfully (SIMULATION PASSED).
```

5. Validating the MIPI D-PHY IP

Validate your hardware using the design example generated from the MIPI D-PHY IP. Validating the MIPI DPHY IP design example requires external loopback from the TX link to the RX link.

1. For external loopback testing with two links on same IO bank, generate one MIPI DPHY IP design example with one TX link and one RX link.

The design example initiates the data from the traffic generator on the TX link to the traffic checker on the RX link.






2. Monitor the test conditions for the example design with Signal Tap Logic Analyzer.

5.1. Adding Signal Tap Logic Analyzer to MIPI D-PHY IP Design Example

Add the Signal Tap logic analyzer to your design to monitor the test results for the MIPI D-PHY IP design example

1. On the **Tools** menu, click **Signal Tap Logic Analyzer**
2. In the **Signal Configuration** window next to the **Clock** box, click ... (**Browse Node Finder**).
3. Select the `clk_splitter_out_clk_clk` from the MIPI D-PHY IP design example
4. Under **Signal Configuration**, specify the following settings:
 - For **Sample depth**, select **512**
 - For **RAM type**, select **Auto**
 - For **Trigger flow control**, select **Sequential**
 - For **Trigger position**, select **Center trigger position**
 - For **Trigger conditions**, select **1**
5. Add the `done` and `fail` signal from the traffic generator instance (`tg_inst`) from the MIPI D-PHY IP design example.

Figure 18. Example for the TX and RX links signals

Tap	Name	5	5	1 ✓ Basic AND
Pre-Syn	dut tg dphy_ppi_tg_inst tg_inst done_link[0]	✓	✓	
Pre-Syn	dut tg dphy_ppi_tg_inst tg_inst done_link[1]	✓	✓	
Pre-Syn	dut tg dphy_ppi_tg_inst tg_inst done	✓	✓	
Pre-Syn	dut tg dphy_ppi_tg_inst tg_inst fail_link[1]	✓	✓	
Pre-Syn	dut tg dphy_ppi_tg_inst tg_inst fail	✓	✓	

6. Save the Signal Tap file by selecting **File ► Save**
7. Select **Yes** on the message of **Do you want to enable Signal tap file "<name>.stp" for the current project?**
8. Run a full design compilation to generate the `.sof` file.

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5.2. Testing the MIPI D-PHY Design Example

You monitor the `done` signal that is asserted in the Signal Tap logic analyzer. You test the external loopback for one TX link to one RX link on the same bank in the same board.

1. Program your board with the design `.sof` file.
2. Run the the Signal Tap logic analyzer to capture the signals without any triggering condition.
3. Check the Signal Tap logic analyzer results to ensure the `done` signals are asserted and the `fail` signals are not asserted



6. Debugging the MIPI-PHY IP

Before debugging your design, confirm that it follows the recommended design flow in the *MIPI D-PHY Interface Design Guidelines* chapter of this user guide. Always keep a record of tests, to avoid repeating the same tests later.

1. Consult the debugging checklist.
 - Try a different fit
 - Ensure you have constrained your design with correct timing constraints and the design timing is closed.
 - Ensure the PLL is locked
 - Measure the power distribution network
 - Measure the signal integrity
 - Measure the FPGA voltages
 - Vary the voltages
 - Heat and cool the PCB
 - Operate the design at lower and higher frequencies
 - Check the PLL clock source, specification and jitter

6.1. Creating a Simplified Design that Demonstrates the Same Problem

To help debugging, create a simple design that replicates the problem. A simple design should compile quickly and be easy to understand. The MIPI D-PHY IP generates an example top-level file that is ideal for debugging. The example top-level file uses all the same parameters and pin-outs.

6.2. Evaluating FPGA Timing Problems

Usually, you should not encounter timing problems with Altera IP unless your design exceeds Altera published performance ranges or you are using a device for which the Quartus Prime software offers only preliminary timing model support. Timing problems may occur if the incorrect constraint are added to .sdc files for the Quartus Prime project

6.3. Determining if the Problem Exists in Previous Quartus Prime Versions

Hardware that works before an update to either the Quartus Prime software or the IP indicates that the development platform is not the issue. However, the previous generation IP may be less susceptible to a PCB problem, masking the problem.

6.4. Determining if the Problem Exists in the Current Version of Software

Determine if the problem still exists in the latest version of the Altera software. Altera add enhancements to and fix bugs in the IP every release. Depending on the nature of the bug or enhancement, it may not always be documented in the release notes.

If the latest version of the software solves the problem, it may be easier to debug the version of software that you are using.

6.5. Verifying the MIPI D-PHY IP Using the Signal Tap Logic Analyzer

The Signal Tap logic analyzer shows read and write activity in the system.

1. On the **Tools** menu, click **Signal Tap Logic Analyzer**.
2. In the **Signal Configuration** window next to the **Clock** box, click ... (**Browse Node Finder**).
3. Type the memory interface system clock in the **Named** box, for **Filter** select **Signal Tap: presynthesis** and click **Search**.
4. Select the memory interface clock that is exposed to the user logic.
5. Click **OK**.
6. Under **Signal Configuration**, specify the following settings:
 - For **Sample depth**, select **512**
 - For **RAM type**, select **Auto**
 - For **Trigger flow control**, select **Sequential**
 - For **Trigger position**, select **Center trigger position**
 - For **Trigger conditions**, select **1**

6.6. Varying the Voltage

Vary the voltage of your system, if you suspect a marginality problem. Increasing the voltage usually causes devices to operate faster and also usually provides increased noise margin.

6.7. Operating at Lower Speed

Test the interface at a lower speed. If the interface works at a lower speed, the interface has correct pin outs and is functional.

6.8. Trying a Different PCB

If you are using the same Altera FPGA IP on several different hardware platforms, determine whether the problem occurs on all platforms or just on one.

Multiple instances of the same PCB, or multiple instances of the same interface, on physically different hardware platforms may exhibit different behavior.

1. Determine if the configuration is fundamentally not working, or if some form of marginality is involved in the problem.
2. If the IP is from a previous project to help save development resources, determine whether the specific IP configuration works on a previous platform.

7. MIPI D-PHY Architecture

The Agilex 3 and Agilex 5 devices implement the MIPI D-PHY IP through HSIO banks. Each HSIO bank consists of 8 byte blocks to support MIPI D-PHY IP. However, one byte blocks is reserved for RZQ calibration and reference clock. Therefore the maximum MIPI D-PHY interfaces that a single HSIO bank can support is up to 7 interfaces (subject to D-PHY lanes configuration). Both the Agilex 3 and Agilex 5 devices offer a native D-PHY interface that allows direct point-to-point connection between the D-PHY transmitter and D-PHY receiver without any passive circuitry or third-party component in between. Each interface can support 1, 2, 4, or 8 data lanes plus 1 clock lane.

Figure 19. MIPI D-PHY IP TX Data and Clock Lane Placement

The figure shows each interface has prefixed data lane and clock lane placement. Refer to the [MIPI D-PHY Interface Implementation](#) section to understand the implementation and how to identify the physical pin placement.

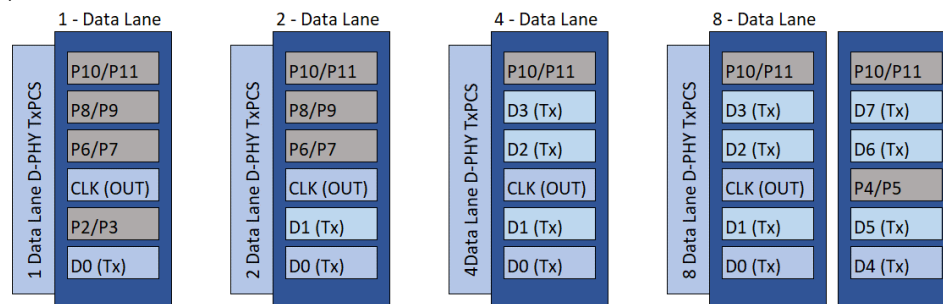
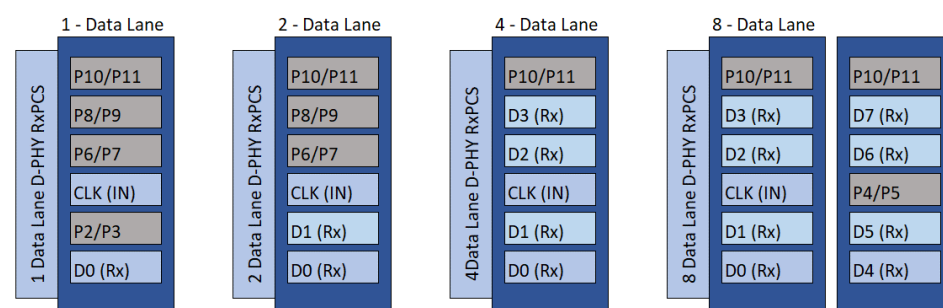


Figure 20. MIPI D-PHY IP RX Data and Clock Lane Placement



7.1. MIPI D-PHY IP TX

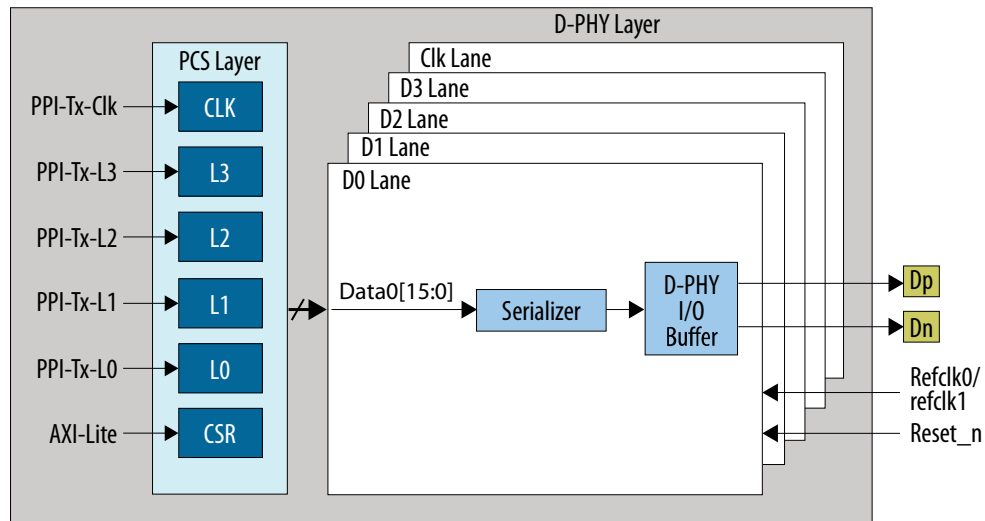
The MIPI D-PHY IP TX architecture includes the following blocks:

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- D-PHY layer. This block handles the PPI data serialization with its clocking scheme and the I/O buffers for HS and LP.
- Physical coding sub-layer (PCS). Processes the PPI and controls the PHY layer operation including the event between high speed (HS) and low power (LP), D-PHY block initialization and calibration.
- AXI-Lite. This optional interface controls the protocol timers and registers.

Figure 21. MIPI D-PHY TX Architecture

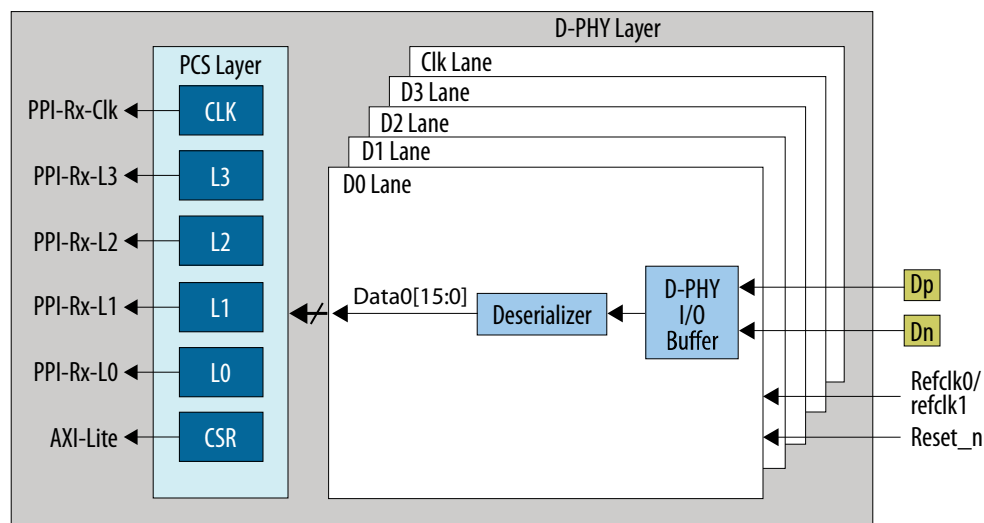


7.2. MIPI D-PHY IP RX

The MIPI D-PHY IP RX architecture includes the following blocks:

- D-PHY layer. This block handles the external incoming data deserialization with its clocking for both HS and LP modes.
- Physical coding sub-layer (PCS). Processes the PPI and controls the PHY layer operation including the event between high speed (HS) and low power (LP), D-PHY block initialization and calibration.
- AXI-Lite. This optional interface controls the protocol timers and registers.

Figure 22. MIPI D-PHY RX Architecture



7.3. Initialization and Reset Sequences

After device power-up and configuration, the D-PHY hard circuitry and soft IP is initialized.

An asynchronous system reset is required to initialize the PCS soft logic to a known good state. This system reset is internally gated with the PLL lock signal to guarantee that the logic comes out of reset only when the clocks are stable, and the following conditions are met:

1. PLL achieves LOCK.
2. INIT_DONE is asserted.
3. PPI.Enable for the active lanes are asserted.
4. Register D-PHY_CSR.Enable is set to '1' (DEFAULT).

The D-PHY IP has a programmable register t_{INIT} that allows the soft IP to implement the initialization sequence. The initialization states for both the D-PHY TX and RX mode are as follows:

Table 17. Initialization States for TX and RX Modes

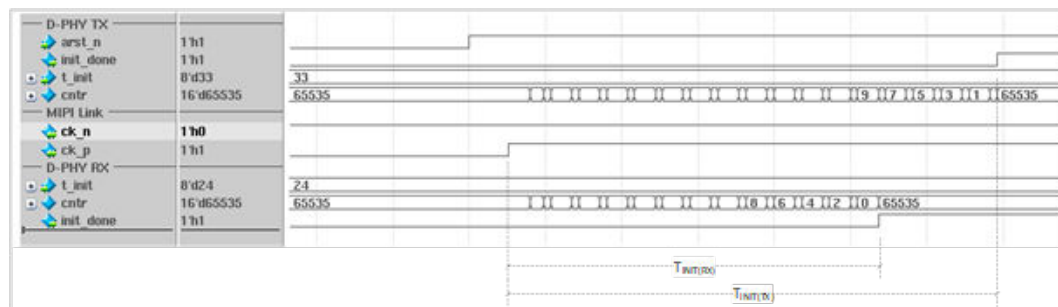
Mode	State	Exit State	Exit Condition	Line Levels
TX	OFF/RESET	TX_INIT	Reset_n deasserted & PLL locked & PPI Enabled .	Not LP-11
TX	TX_INIT	TX_READY	A first stop state for a period longer than t_{INIT} timeout as specified by the protocol. Init_done is asserted	LP-11
TX	TX_READY	RESET	Reset_n asserted or PLL unlocked or PPI disabled	Active
continued...				

Mode	State	Exit State	Exit Condition	Line Levels
RX	OFF/RESET	RX_INIT	Reset_n deasserted & PLL locked & PPI Enabled	Any
RX	RX_INIT	RX_READY	Observe LP11 for t_{INIT}	LP-11
RX	RX_READY	RESET	Reset_n asserted or PLL unlocked or PPI disabled	Active

The RX D-PHY is initialized when the TX D-PHY drives a stop state (LP-11) for a period longer than T_{INIT} . The first stop state longer than the specified T_{INIT} is called the initialization period. The TX D-PHY itself shall be initialized by a system or protocol input signal (PPI).

The following is a timing diagram for the initialization sequence for both D-PHY TX and D-PHY RX modes.

Figure 23. Initialization Sequence Timing Diagram



Each clock domain has both a synchronous and asynchronous reset. These signals are generated internally from the incoming system reset (gated with PLL lock) and D-PHY link's PPI.Enable signal for data lane 0 properly synchronized to the destination clock domains.

The register interface uses the synchronous reset input port `srst_axil_n`. This reset domain is totally independent of the rest of the logic with no dependency on the system reset, PLL lock or `init_done` signals.

7.4. Calibration

The MIPI D-PHY IP provides the following types of calibration:

- Initial skew calibration
 - Required for bit rate > 1.5 Gbps; optional for bit rates below 1.5 Gbps.
 - Data pattern used is 1010... clock pattern.
 - Minimum duration of 20^{15} UI (maximum at 100 us)

- Alternate calibration
 - Required for bit rate > 2.5 Gbps; optional for bit rates below 2.5 Gbps .
 - Data pattern used in PRBS9.
 - Minimum duration of 20^{15} UI (maximum at 100 us).
- Periodic skew calibration
 - Optional at any bit rate.
 - Data pattern used is 1010...
 - Minimum duration of 2^{10} UIs (maximum of 10 us).
- Preamble
 - Required for bit rate > 2.5 Gbps; optional for bit rates below 2.5 Gbps.
 - Preamble data pattern of 1010... precedes every HS data packet.
 - Minimum duration of 32 UI (max of 512 UI).

Table 18. D-PHY IP Calibration Support Matrix

Calibration Type	Support	Comment
Initial skew calibration	Supported	MIPI D-PHY IP configurable Rx: Adjust clock delay to center data window Tx: Auto calibration logic starts when all lanes go to INIT done state calibration (protocol side can also initiate this using PPI. TxSkewCalHS)
Alternate calibration	Supported	MIPI D-PHY IP configurable Rx: Adjust clock delay to center data window; determine data dependent window edge shifts Tx: Auto calibration logic starts after initial skew calibration (protocol side can also initiate this using PPI.TxAlternateCalHS)
Periodic skew calibration	Supported	MIPI D-PHY IP configurable Rx: Minor adjustment on window edges Tx: Protocol controlled (using PPI.TxSkewCalHS)
Preamble	Supported	MIPI D-PHY IP configurable Rx: recognize preamble but will not make any adjustments Tx: automatically inserts PREAMBLE for every HS transfer

7.5. CSR Clock Domain Crossing (CDC)

The D-PHY IP has a few clock domain crossings. The most major one is between the regfile's `axi_clk` and the rest of the D-PHY PCS.

Most of the control registers from the regfile CSR are not synchronized to the destination clock domains. To ensure proper synchronization, observe the following sequence when updating any control registers (this excludes clearing status registers):

1. Disable D-PHY by writing a 0 to `D-PHY_CSR.Enable` (offset 0x10 bit 0).
2. Update control registers.
3. Enable D-PHY by writing a 1 to `D-PHY_CSR.Enable` (offset 0x10 bit 0).

Alternatively, to use the link's data lane 0's `PPI.Enable` signal to reset the D-PHY link when updating the control registers.



8. Interface Signals and Register Maps

8.1. Interface Signals

After you have instantiated and parameterized your MIPI D-PHY IP, the following signals ports are available.

8.1.1. General Interface Signals

Table 19. General Interface Signals

Signal	Direction	Width	Description
LINK n _D-PHY_link_cp	TX - output RX - input	1	D-PHY clock lane pins for link n .
LINK n _D-PHY_link_cn			
LINK n _D-PHY_link_dp	TX - output RX - input	m	D-PHY data lane pins for link n (where m is the number of data lanes = 1,2,4 or 8).
LINK n _D-PHY_link_dn			
arst_n	input	1	Asynchronous system reset (low-asserted).
LINK n _link_core_clk	output	1	Core clock for Link n .
LINK n _link_srst_n	output	1	Sync reset for Link n (low-asserted).
LINK n _link_arst_n	output	1	Async reset for Link n (low-asserted).
ref_clk_0_p	input	1	Reference clock input for PLL 0. Ref_clk_0_n is only required when using true differential signaling.
ref_clk_0_n			
ref_clk_1_p	input	1	Reference clock input for PLL 1 when used. Ref_clk_1_n is only required when using true differential signaling.
ref_clk_1_n			
rzq	input	1	RZQ pin used for OCT calibration. Refer to the MIPI D-PHY Interface Implementation section for implementation details.

8.1.2. AXI-Lite Interface

The D-PHY IP allows AXI-Lite bus to access the CSR of the D-PHY.

Aside from allowing access to the D-PHY internal IP registers, the AXI-Lite bus is designed to allow access to external registers which is used for accessing the PPI TG. The following shows the AXI-Lite signal port and function. For details of the AXI-Lite internal memory map, refer to the tables in the [AXI-Lite CSR Access](#) topic.

Table 20. AXI-Lite Interface Signals

Signal	Direction	Width	Description
axil_clk	Input	1	AXI-Lite clock.
srst_axil_n	Input	1	AXI_lite synchronous reset.
axi_lite_awaddr	Input	12	Write address.
axi_lite_awvalid	Input	1	Write address valid. This signal indicates that the channel is signaling valid write address and control information.
axi_lite_awready	Output	1	Write address ready. This signal indicates that the slave is ready to accept an address and associated control signals.
axi_lite_wdata	Input	32	Write data.
axi_lite_wstrb	Input	4	Write strobes. This signal indicates which byte lanes hold valid data. There is one write strobe bit for each eight bits of the write data bus.
axi_lite_wvalid	Input	1	Write valid. This signal indicates that valid write data and strobes are available.
axi_lite_wready	Output	1	Write ready. This signal indicates that the slave can accept the write data.
axi_lite_bresp	Output	2	Write data.
axi_lite_bvalid	Output	1	Write response valid. This signal indicates that the channel is signaling a valid write response.
axi_lite_bready	Input	1	Response ready. This signal indicates that the master can accept a write response
axi_lite_araddr	Input	12	Read address.
axi_lite_arvalid	Input	1	Read address valid. This signal indicates that the channel is signaling valid read address and control information.
axi_lite_arready	Output	1	Read address ready. This signal indicates that the slave is ready to accept an address and associated control signals.
axi_lite_rdata	Output	32	Read data.
axi_lite_rresp	Output	2	Read response. This signal indicates the status of the read transfer.
axi_lite_rvalid	output	1	Read valid. This signal indicates that the channel is signaling the required read data.
axi_lite_rready	Input	1	Read ready. This signal indicates that the master can accept the read data and response information.
axi_lite_arprot	Input	3	Unused.
axi_lite_awprot	Input	3	Unused.

8.1.3. Core Register Bus

The D-PHY IP allows the AXI-Lite client bus interface to be shared with an external IP to conserve resources.

A typical use-case would be the connection of the TG block. The TG block does not require any AXI-Lite interface, just a simple register bus defined below.

Table 21. Core Register Interface

Signal	Direction	Width	Description
reg_wr_en_o	Output	1	Register write enable.
reg_rd_en_o	Output	1	Register read enable.
reg_raddr_o	Output	11	Read address.
reg_waddr_o	Output	11	Write address.
reg_be_o	Output	4	Byte enables.
reg_din_o	Output	32	Write data input.
reg_dout_i	Input	32	Read data output.

8.1.4. D-PHY RX PPI Interface Signals

These PPI interface signals are used only when the D-PHY IP is configured for receive (RX). Each lane (clock and data) of each link has a PPI RX interface attached to it.

Figure 24. PPI Interface Signals

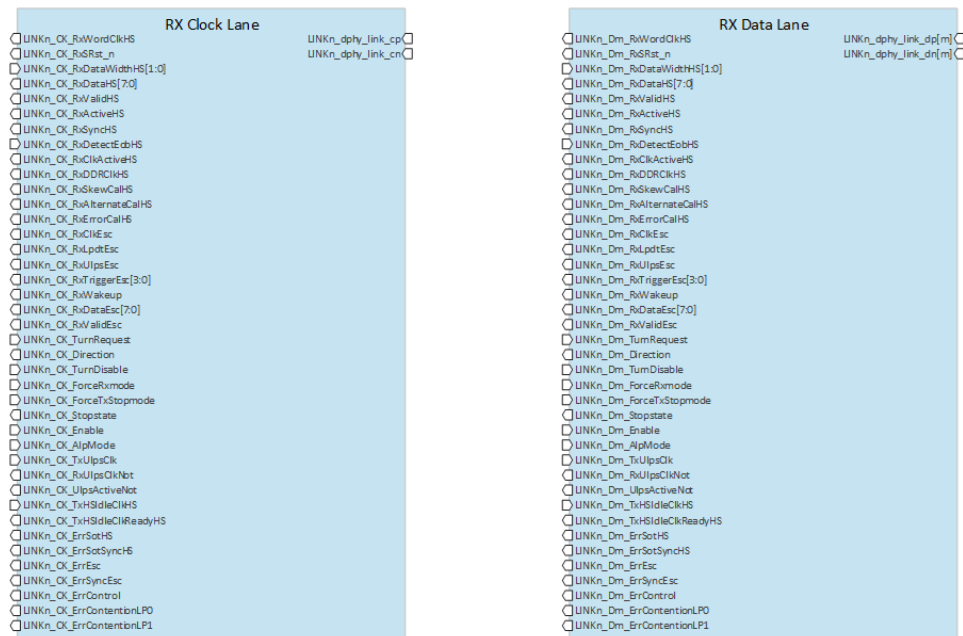


Table 22. PPI RX Interface - Link *n*, Clock Lane

Signal	Direction	Width	Description
High-Speed Receive Signals (Link <i>n</i>, Clock Lane) - RX only			
LINKnn_CK_RxWordClkHS	Output	1	High-Speed Receive Word Clock (link <i>n</i> , clock lane) This is used to synchronize signals in the high-speed receive clock domain.
<i>continued...</i>			

Signal	Direction	Width	Description
			<p>The RxWordClkHS is generated by dividing the recovered high-speed clock. The frequency of RxWordClkHS is dependent upon the width of the High-Speed Receive Data, as follows:</p> <ul style="list-style-type: none"> 16-bit width, RxDataHS[15:0], the High-Speed Receive Word Clock is exactly 1/16 the high-speed received data rate. <p>For links with multiple data Lanes, the PHY implements one RxWordClkHS signal per lane.</p>
LINKn_CK_RxSRst_n	Output	1	Link Sync Reset (link n, clock lane). Link synchronous reset (synchronized to Linkn_CK_RxWordClkHS).
LINKn_CK_RxDataWidthHS	Input	2	<p>High-Speed Receive Data Width Select (link n, clock lane). Selects the bus width of RxDataHS:</p> <ul style="list-style-type: none"> RxDataWidthHS[1:0] = 00: not used, reserved RxDataWidthHS[1:0] = 01: 16-bit, RxDataHS[15:0] RxDataWidthHS[1:0] = 10 : not used, reserved RxDataWidthHS[1:0] = 11: not used, reserved. <p>An implementation may support any data width - one fixed width, or subset of widths or all widths defined above.</p>
LINKn_CK_RxDataHS	Output	8	High-Speed Receive Data (link n, clock lane).
LINKn_CK_RxValidHS	Output	1	High-Speed Receive Data Valid (link n, clock lane.)
LINKn_CK_RxActiveHS	Output	1	<p>High-Speed Reception Active (link n, clock lane)</p> <p>This active high signal indicates that the Lane Module is actively receiving a High-Speed transmission from the Lane interconnect. There is no timing relationship between Stopstate being deasserted and RxActiveHS being asserted. Likewise, there is no relationship between Stopstate being asserted and RxActiveHS being deasserted. When receiving any high speed data transfer including Alternate Calibration or high speed deskew pattern, RxActiveHS is asserted.</p>
LINKn_CK_RxSyncHS	Output	1	Receiver Synchronization Observed (link n, clock lane).
LINKn_CK_RxDetectEobHS	Input	1	Receiver Detection Of End Of Burst (link n, clock lane).
LINKn_CK_RxCikActiveHS	Output	1	<p>Receiver Clock Active (link n, clock lane)</p> <p>This asynchronous, active high signal indicates that a Clock Lane is receiving a DDR Clock signal. There is no timing relationship between Stopstate being deasserted and RxCikActiveHS being asserted. Likewise, there is no relationship between Stopstate being asserted and RxCikActiveHS being deasserted.</p>
LINKn_CK_RxDDRCikHS	Output	1	Receiver DDR Clock (link n, clock lane).
LINKn_CK_RxSkewCalHS	Output	1	High-Speed Receive Skew Calibration (link n, clock lane).
LINKn_CK_RxAlternateCalHS	Output	1	High-Speed Receive Alternate Calibration Sequence (link n, clock lane).
continued...			

Signal	Direction	Width	Description
LINKn_CK_RxErrorCalHS	Output	1	High-Speed Receive Calibration Error (link n, clock lane) .
Escape Mode Receive Signals (Link n, Clock Lane) - RX only			
LINKn_CK_RxCikEsc	Output	1	Escape Mode Receive Clock (link n, clock lane) This signal is used to transfer received data to the protocol during LP mode and ALP mode. In LP mode, this signal is generated from the two Low-Power signals in the Lane interconnect. Because of the asynchronous nature of Escape Mode data transmission, this signal may not be periodic. The number of pulses of this signal is limited to the activity on the lines, so it is advisable that this signal not be used as clock for the protocol layer. In ALP mode, this clock is generated by dividing the recovered high-speed clock, and is exactly 1/8 the high-speed received data rate.
LINKn_CK_RxLpdtEsc	Output	1	Escape Low-Power Data Receive mode (link n, clock lane).
LINKn_CK_RxUlpsEsc	Output	1	Escape Ultra-Low Power (Receive) mode (link n, clock lane) This active high signal is asserted to indicate that the Lane Module has entered the Ultra-Low Power State, due to the detection of a received ULPS command. The Lane Module remains in this mode with RxUlpsEsc asserted until a Stop state is detected on the Lane interconnect.
LINKn_CK_RxTriggerEsc	Output	4	Escape Mode Receive Trigger 0-3 (link n, clock lane).
LINKn_CK_RxWakeup	Output	1	Receiver Wakeup Pulse Detected (link n, clock lane) For ALP mode implementations, this active high signal indicates that a wakeup pulse (ALP-01) is currently being detected. This signal is driven directly from the analog ALP wakeup detector and is not timed to any PPI signal.
LINKn_CK_RxDataEsc	Output	8	Escape Mode Receive Data (link n, clock lane).
LINKn_CK_RxValidEsc	Output	1	Escape Mode Receive Data Valid (link n, clock lane).
Control Signals (Link n, Clock Lane)			
LINKn_CK_TurnRequest	Input	1	Turnaround Request (link n, clock lane).
LINKn_CK_Direction	Output	1	Transmit/Receive Direction (link n, clock lane) This signal is used to indicate the current direction of the Lane interconnect. <ul style="list-style-type: none"> When Direction=0, the Lane is in transmit mode (0=Output). When Direction=1, the Lane is in receive mode (1=Input). When transitioning from TX to RX, the direction changes state after completion of a successful BTA procedure, as indicated by the detection of Mark-1 followed by LP-11. When transitioning from RX to TX, the direction changes state after the TTA-SURE time has been met, and the local driver starts transmitting LP-00.
<i>continued...</i>			

Signal	Direction	Width	Description
			Any abnormalities during the BTA procedure can result in contention conditions, requiring the protocol layer to implement mechanisms to detect and resolve.
LINKn_CK_TurnDisable	Input	1	Disable Turnaround (link n, clock lane).
LINKn_CK_ForceRxmode	Input	1	<p>Force Lane Module Into Receive mode / Wait for Stop state (link n, clock lane) - RX only</p> <p>This signal allows the protocol to initialize a Lane Module, or force a Bi-directional Lane Module, into receive mode. This signal is used during initialization or to resolve a contention situation. When this signal is high, the Lane Module immediately transitions into receive Control mode and waits for a Stop state to appear on the Lane interconnect.</p> <p>When used for initialization, this signal will be released (i.e., driven low) only when the Dp Dn inputs are in Stop state for a time T_{INIT}, or longer. The assertion of ForceRxmode and ForceTxStopmode are mutually exclusive.</p>
LINKn_CK_ForceTxStopmode	Input	1	<p>Force Lane Module Into Transmit mode / Generate Stop state (link n, clock lane) - TX only</p> <p>This signal allows the protocol to force a Lane Module into transmit mode and Stop state during initialization or following an error situation, e.g. expired time out. When this signal is high, the Lane Module immediately transitions into transmit mode and the module state machine is forced into the Stop state. The protocol layer does not assert TxRequestEsc, TxRequestHS, or Turnrequest for an implementation-specific period of time after the deassertion of ForceTxStopMode, in order to create a safe margin for the PHY to be able to accept a new request.</p> <p>The assertion of ForceRxmode and ForceTxStopmode are mutually exclusive.</p>
LINKn_CK_Stopstate	Output	1	<p>Lane is in Stop state (link n, clock lane)</p> <p>This active high signal indicates that the Lane Module, regardless of whether the Lane Module is a transmitter or a receiver, is currently in Stop state. This indicates that the PHY Line levels are in the LP-11 state, and the PHY state machine is in the stop state and ready to receive a request for the next operation. Also, the protocol may use this signal to indirectly determine if the PHY Line levels are in the LP-11 state. A Master will not assert this signal during initialization until after LP-11 has been driven for the required T_{INIT} time. A Slave will not assert this signal during initialization until after LP-11 has been detected for the required T_{INIT} time.</p>
LINKn_CK_Enable	Input	1	<p>Enable Lane Module (link n, clock lane)</p> <p>This active high signal forces the Lane Module out of "shutdown". All Line drivers, receivers, terminators, and contention detectors are turned off when Enable is low. Furthermore, while Enable is low, all other PPI inputs are ignored, and all PPI outputs are driven to the default inactive state. Enable is a level sensitive signal and does not depend on any clock.</p>
continued...			

Signal	Direction	Width	Description
LINKn_CK_AlpMode	Input	1	Alternate Low Power Mode Selection (link n, clock lane).
LINKn_CK_TxUlpClk	Input	1	Transmit Ultra-Low Power State on Clock Lane (link n, clock lane) - TX only This active-high signal is asserted to cause a Clock Lane Module to enter the Ultra-Low Power State. The Lane Module remains in this mode until TxUlpClk is de-asserted.
LINKn_CK_RxUlpClkNot	Output	1	Receive Ultra-Low Power State on Clock Lane (link n, clock lane) - RX only This active low signal is asserted to indicate that the Clock Lane Module has entered the Ultra-Low Power State due to the detection of a request to enter the ULP state. The Lane Module remains in this mode with RxUlpClkNot asserted until a Stop state is detected on the Lane Interconnect.
LINKn_CK_UlpActiveNot	Output	1	ULP State (not) Active (link n, clock lane) This active low signal is asserted to indicate that the Lane is in ULP state. For a transmitter, this signal is asserted some time after TxUlpEsc and TxRequestEsc (TxUlpClk for a Clock Lane) are asserted. The transmitting PHY continues to supply TxClkEsc until UlpActiveNot is asserted. To leave ULP state, the transmitter first drives TxUlpExit high, then waits for UlpActiveNot to become high (inactive). At that point, the transmitting PHY is active and has started transmitting a Mark-1 on the Lines. The protocol waits for a time Twakeup and then drives TxRequestEsc (TxUlpClk) inactive to return the Lane to Stop state. For a receiver, this signal indicates that the Lane is in ULP state. When entering the ULP state, RxUlpEsc (or RxUlpClkNot for a Clock Lane) is asserted to indicate the detection of the ULPS command and entry into the ULP state, followed by the assertion of the UlpActiveNot, indicating that the PHY is in the ULP state. When exiting the ULP state, this signal is deasserted to indicate that the PHY has detected a Mark-1 to initiate the exit from the ULP state. After the required TWAKEUP, the RxUlpEsc, or RxUlpClkNot for a Clock Lane, is deasserted to indicate the PHY has exited the ULP state and LP-11 has been detected.
LINKn_CK_TxHSIdleClkHS	Input	1	HS-Idle State Start (link n, clock lane).
LINKn_CK_TxHSIdleClkReadyHS	Output	1	Clock Ready to Exit HS-Idle-ClkHS0 Sub-State (link n, clock lane).
Error Signals (Link n, Clock Lane) - RX only			
LINKn_CK_ErrSoTHS	Output	1	Start-of-Transmission (SoT) Error (link n, clock lane).
LINKn_CK_ErrSotSyncHS	Output	1	Start-of-Transmission Synchronization Error (link n, clock lane).
LINKn_CK_ErrEsc	Output	1	Escape Entry Error (link n, clock lane).
LINKn_CK_ErrSyncEsc	Output	1	Low-Power Data Transmission Synchronization Error (link n, clock lane).
LINKn_CK_ErrControl	Output	1	Control Error (link n, clock lane)
continued...			

Signal	Direction	Width	Description
			This active high signal is asserted when an incorrect Line state sequence is detected in LP and ALP modes. Once asserted, this signal remains asserted until the next transaction starts, so that the protocol can properly process the error. Section A.18 describes the LP and ALP signaling error sequences that require this signal to be asserted, as well as error sequences that can optionally result in this signal being asserted. Sequences that can optionally result in this signal being asserted are implementation specific.
LINKn_CK_ErrContentionLP0	Output	1	LP0 Contention Error (link n, clock lane).
LINKn_CK_ErrContentionLP1	Output	1	LP1 Contention Error (link n, clock lane).

Table 23. PPI RX Interface – Link n, Data Lane m

Signal	Direction	Width	Description
High-Speed Receive Signals (Link n, Data Lane m) - RX only			
LINKn_Dm_RxWordClkHS	Output	1	<p>High-Speed Receive Word Clock (link n, data lane m)</p> <p>This signal synchronizes signals in the high-speed receive clock domain. The RxWordClkHS is generated by dividing the recovered high-speed clock. The frequency of RxWordClkHS is dependent upon the width of the High-Speed Receive Data, as follows:</p> <ul style="list-style-type: none"> 16-bit width, RxDataHS[15:0], the High-Speed Receive Word Clock is exactly 1/16 the high-speed received data rate. <p>For links with multiple data Lanes, the PHY implements one RxWordClkHS signal per lane.</p>
LINKn_Dm_RxSRst_n	Output	1	Link Sync Reset (link n, data lane m) Link synchronous reset (synchronized to Linkn_CK_RxWordClkHS).
LINKn_Dm_RxDataWidthHS	Input	2	<p>High-Speed Receive Data Width Select (link n, data lane m)</p> <p>Selects the bus width of RxDataHS:</p> <ul style="list-style-type: none"> RxDataWidthHS[1:0] = 00: not used, reserved RxDataWidthHS[1:0] = 01: 16-bit, RxDataHS[15:0] RxDataWidthHS[1:0] = 10: not used, reserved RxDataWidthHS[1:0] = 11: not used, reserved. <p>An implementation may support any data width - one fixed width, or subset of widths or all widths defined above.</p>
LINKn_Dm_RxDataHS	Output	8	<p>High-Speed Receive Data (link n, data lane m)</p> <p>High-speed data received by the Lane Module.</p> <p>If the RxValidHS signals indicate that more than 8 bits were received, then the byte reception order over the physical interface is: RxDataHS[7:0] followed by RxDataHS[15:8]. Data is transferred on rising edges of RxWordClkHS.</p> <p>The following signals are defined for the High-Speed Receive Data based on the width of the receive data path:</p> <ul style="list-style-type: none"> 16-bit width – RxDataHS[15:0]
<i>continued...</i>			

Signal	Direction	Width	Description
			An implementation may support any data width - one fixed width, or subset of widths or all widths defined above. The LSB will be received as the first bit and the MSB will be received as the last bit.
LINKn_Dm_RxValidHS	Output	1	<p>High-Speed Receive Data Valid (link n, data lane m)</p> <p>This active high signal indicates that the Lane Module is driving data to the protocol layer on the RxDataHS output. There is no "RxReadyHS" signal, and the protocol layer is expected to capture RxDataHS on every rising edge of RxWordClkHS where any RxValidHS bit is asserted. There is no provision for the protocol layer to slow down ("throttle") the receive data.</p> <p>The following High-Speed Receive Data Valid signals are defined based on the width of the receive data path:</p> <ul style="list-style-type: none"> 16-bit width – RxValidHS[1:0] <p>The following High-Speed Receive Data Valid signals indicate which bits of the RxDataHS data bus contain valid data as follows:</p> <ul style="list-style-type: none"> RxValidHS[0] – RxDataHS[7:0] contains valid data that was received from the channel. RxValidHS[1] – RxDataHS[15:8] contains valid data that was received from the channel. <p>For links with more than one data Lane, it is possible that each data Lane's RxValidHS low-to-high and high-to-low transition may be in a different RxWordClkHS cycle.</p> <p>RxValidHS is not asserted for high speed deskew bursts or alternate calibration sequences.</p> <p>RxValidHS is not asserted if ErrSotSyncHS is asserted. If the PHY does not support EOT processing, all bits of RxValidHS[1:0] are asserted when there is valid data received from the channel.</p>
LINKn_Dm_RxActiveHS	Output	1	<p>High-Speed Reception Active (link n, data lane m)</p> <p>This active high signal indicates that the Lane Module is actively receiving a High-Speed transmission from the Lane interconnect. There is no timing relationship between Stopstate being deasserted and RxActiveHS being asserted.</p> <p>Likewise, there is no relationship between Stopstate being asserted and RxActiveHS being deasserted. When receiving any high speed data transfer including Alternate Calibration or high speed deskew pattern, RxActiveHS is asserted.</p>
LINKn_Dm_RxSyncHS	Output	1	<p>Receiver Synchronization Observed (link n, data lane m)</p> <p>This active-high signal indicates that the Lane Module has seen an appropriate synchronization event.</p> <p>In a typical High-Speed transmission, RxSyncHS is high for one cycle of RxWordClkHS at the beginning of a High-Speed transmission when RxActiveHS is first asserted. RxSyncHS is asserted even if ErrSothHS is asserted. RxSyncHS is not asserted if ErrSotSyncHS is asserted.</p>
LINKn_Dm_RxDetectEobHS	Input	1	Receiver Detection Of End Of Burst (link n, data lane m).
LINKn_Dm_RxCkActiveHS	Output	1	Receiver Clock Active (link n, data lane m)
continued...			

Signal	Direction	Width	Description
			This asynchronous, active high signal indicates that a Clock Lane is receiving a DDR Clock signal. There is no timing relationship between Stopstate being deasserted and RxClkActiveHS being asserted. Likewise, there is no relationship between Stopstate being asserted and RxClkActiveHS being deasserted.
LINKn_Dm_RxDDRCIkHS	Output	1	Receiver DDR Clock (link n, data lane m).
LINKn_Dm_RxSkewCalHS	Output	1	High-Speed Receive Skew Calibration (link n, data lane m) This optional active-high signal indicates that the high speed deskew burst is being received. RxSkewCalHS is set to the active state when the all-ones sync pattern is received, and is cleared to the inactive state when Dp and Dn transition back to the LP-11 Stop State. RxSkewCalHS is not asserted for the Alternate Calibration Sequence.
LINKn_Dm_RxAlternateCalHS	Output	1	High-Speed Receive Alternate Calibration Sequence (link n, data lane m) This optional active-high signal indicates that the alternate Calibration Sequence is being received. RxAlternateCalHS is set to the active state when the "11110000" sync pattern is received, and is cleared to the inactive state when Dp and Dn transition back to the LP-11 Stop State.
LINKn_Dm_RxErrorCalHS	Output	1	High-Speed Receive Calibration Error (link n, data lane m) This optional asynchronous active-high signal indicates that the high speed calibration ended with errors. This signal is asserted if the initial deskew calibration (RxSkewCalHS is asserted) or alternate calibration (RxAlternateCalHS is asserted) has not completed successfully. If it is asserted in any of the initial calibrations, proper received data cannot be expected, and the system takes an implementation-specific action to resolve the condition. This signal can also be asserted if periodic deskew (RxSkewCalHS is asserted) or preamble sequence did not complete successfully. It is implementation-specific how the system responds to this condition. RxErrorCalHS signal continues to be asserted until a new calibration sequence is received, or the PHY is disabled and re-enabled.
Escape Mode Receive Signals (Link n, Data Lane m) - RX only			
LINKn_Dm_RxClkEsc	Output	1	Escape Mode Receive Clock (link n, data lane m) This signal transfers received data to the protocol during LP mode and ALP mode. In LP mode, this signal is generated from the two Low-Power signals in the Lane interconnect. Because of the asynchronous nature of Escape Mode data transmission, this signal may not be periodic. The number of pulses of this signal is limited to the activity on the lines, so it is advisable that this signal not be used as clock for the protocol layer. In ALP mode, this clock is generated by dividing the recovered high-speed clock, and is exactly 1/8 the high-speed received data rate.
continued...			

Signal	Direction	Width	Description
LINKn_Dm_RxLpdtEsc	Output	1	<p>Escape Low-Power Data Receive mode (link n, data lane m) - Data lane 0 only</p> <p>This active-high signal is asserted to indicate that the Lane Module is in Low-Power data receive mode. While in this mode, received data bytes are driven onto the RxDataEsc output when RxValidEsc is active. The Lane Module remains in this mode with RxLpdtEsc asserted until a Stop state is detected on the Lane interconnect.</p>
LINKn_Dm_RxUlpsEsc	Output	1	<p>Escape Ultra-Low Power (Receive) mode (link n, data lane m)</p> <p>This active-high signal is asserted to indicate that the Lane Module has entered the Ultra-Low Power State, due to the detection of a received ULPS command. The Lane Module remains in this mode with RxUlpsEsc asserted until a Stop state is detected on the Lane interconnect.</p>
LINKn_Dm_RxTriggerEsc	Output	4	<p>Escape Mode Receive Trigger 0-3 (link n, data lane m)</p> <p>These active-high signals indicate that a trigger event has been received.</p> <p>The asserted RxTriggerEsc signal remains active until a Stop state is detected on the Lane interconnect.</p> <p>RxTriggerEsc[0] corresponds to Reset-Trigger.</p> <p>RxTriggerEsc[1] corresponds to Entry sequence for HS Test mode Trigger.</p> <p>RxTriggerEsc[2] corresponds to Unknown-4 Trigger.</p> <p>RxTriggerEsc[3] corresponds to Unknown-5 Trigger.</p>
LINKn_Dm_RxWakeup	Output	1	<p>Receiver Wakeup Pulse Detected (link n, data lane m)</p> <p>For ALP mode implementations, this active high signal indicates that a wakeup pulse (ALP-01) is currently being detected. This signal is driven directly from the analog ALP wakeup detector and is not timed to any PPI signal.</p>
LINKn_Dm_RxDataEsc	Output	8	<p>Escape Mode Receive Data (link n, data lane m) - Data lane 0 only</p> <p>This is the eight-bit Escape Mode Low-Power data received by the Lane Module. The signal connected to RxDataEsc[0] was received first. Data is transferred on rising edges of RxClkEsc.</p>
LINKn_Dm_RxValidEsc	Output	1	<p>Escape Mode Receive Data Valid (link n, data lane m) - Data lane 0 only</p> <p>This active-high signal indicates that the Lane Module is driving valid data to the protocol on the RxDataEsc output.</p> <p>There is no "RxReadyEsc" signal, and the protocol is expected to capture RxDataEsc on every rising edge of RxClkEsc where RxValidEsc is asserted.</p> <p>There is no provision for the protocol to slow down ("throttle") the receive data. Control Signals Turnaround Request. This active high signal is used to indicate that the protocol desires to initiate a Bi-directional data Lane Turnaround, to allow the other side to begin transmissions.</p> <p>TurnRequest is valid on rising edge of TxClkEsc. TurnRequest is only meaningful for a Bi-directional data Lane Module that is currently the transmitter (Direction=0). If the Bi-directional data</p>

continued...

Signal	Direction	Width	Description
			Lane Module is in receive mode (Direction=1), this signal is ignored. A low-to-high transition on TurnRequest can only happen when Stopstate is asserted.
Control Signals (Link n, Data Lane m)			
LINKn_Dm_TurnRequest	Input	1	Turnaround Request (link n, data lane m).
LINKn_Dm_Direction	Output	1	<p>Transmit/Receive Direction (link n, data lane m)</p> <p>This signal indicates the current direction of the Lane interconnect.</p> <p>When Direction=0, the Lane is in transmit mode (0=Output).</p> <p>When Direction=1, the Lane is in receive mode (1=Input).</p> <p>When transitioning from TX to RX, the direction changes state after completion of a successful BTA procedure, as indicated by the detection of Mark-1 followed by LP-11.</p> <p>When transitioning from RX to TX, the direction changes state after the TTA-SURE time has been met, and the local driver starts transmitting LP-00.</p> <p>Any abnormalities during the BTA procedure can result in contention conditions, requiring the protocol layer to implement mechanisms to detect and resolve.</p>
LINKn_Dm_TurnDisable	Input	1	Disable Turnaround (link n, data lane m).
LINKn_Dm_ForceRxmode	Input	1	<p>Force Lane Module Into Receive mode / Wait for Stop state (link n, data lane m) - RX only</p> <p>This signal allows the protocol to initialize a Lane Module, or force a Bi-directional Lane Module, into receive mode. This signal is used during initialization or to resolve a contention situation.</p> <p>When this signal is high, the Lane Module immediately transitions into receive Control mode and waits for a Stop state to appear on the Lane interconnect.</p> <p>When used for initialization, this signal is released (i.e., driven low) only when the Dp Dn inputs are in Stop state for a time TINIT, or longer. The assertion of ForceRxmode and ForceTxStopmode are mutually exclusive.</p>
LINKn_Dm_ForceTxStopmode	Input	1	<p>Force Lane Module Into Transmit mode / Generate Stop state (link n, data lane m) - TX only</p> <p>This signal allows the protocol to force a Lane Module into transmit mode and Stop state during initialization or following an error situation, e.g. expired time out.</p> <p>When this signal is high, the Lane Module immediately transitions into transmit mode and the module state machine is forced into the Stop state. The protocol layer does not assert TxRequestEsc, TxRequestHS, or Turnrequest for an implementation-specific period of time after the deassertion of ForceTxStopMode, in order to create a safe margin for the PHY to be able to accept a new request. The assertion of ForceRxmode and ForceTxStopmode are mutually exclusive.</p>
LINKn_Dm_Stopstate	Output	1	Lane is in Stop state (link n, data lane m)
<i>continued...</i>			

Signal	Direction	Width	Description
			<p>This active-high signal indicates that the Lane Module, regardless of whether the Lane Module is a transmitter or a receiver, is currently in Stop state.</p> <p>This indicates that the PHY Line levels are in the LP-11 state, and the PHY state machine is in the stop state and ready to receive a request for the next operation. Also, the protocol may use this signal to indirectly determine if the PHY Line levels are in the LP-11 state.</p> <p>A Master will not assert this signal during initialization until after LP-11 has been driven for the required T_{INIT} time. A Slave will not assert this signal during initialization until after LP-11 has been detected for the required T_{INIT} time.</p>
LINKn_Dm_Enable	Input	1	<p>Enable Lane Module (link n, data lane m)</p> <p>This active-high signal forces the Lane Module out of "shutdown". All Line drivers, receivers, terminators, and contention detectors are turned off when Enable is low. Furthermore, while Enable is low, all other PPI inputs are ignored, and all PPI outputs are driven to the default inactive state. Enable is a level sensitive signal and does not depend on any clock.</p>
LINKn_Dm_AlpMode	Input	1	<p>Alternate Low Power Mode Selection (link n, data lane m).</p>
LINKn_Dm_TxUlpsClk	Input	1	<p>Transmit Ultra-Low Power State on Clock Lane (link n, data lane m) - TX only</p> <p>This active-high signal is asserted to cause a Clock Lane Module to enter the Ultra-Low Power State. The Lane Module remains in this mode until TxUlpsClk is de-asserted.</p>
LINKn_Dm_RxUlpsClkNot	Output	1	<p>Receive Ultra-Low Power State on Clock Lane (link n, data lane m) - RX only</p> <p>This active-low signal is asserted to indicate that the Clock Lane Module has entered the Ultra-Low Power State due to the detection of a request to enter the ULP state. The Lane Module remains in this mode with RxUlpsClkNot asserted until a Stop state is detected on the Lane Interconnect.</p>
LINKn_Dm_UlpsActiveNot	Output	1	<p>ULP State (not) Active (link n, data lane m)</p> <p>This active-low signal is asserted to indicate that the Lane is in ULP state.</p> <p>For a transmitter, this signal is asserted some time after TxUlpsEsc and TxRequestEsc (TxUlpsClk for a Clock Lane) are asserted. The transmitting PHY continues to supply TxClkEsc until UlpsActiveNot is asserted. In order to leave ULP state, the transmitter first drives TxUlpsExit high, then waits for UlpsActiveNot to become high (inactive). At that point, the transmitting PHY is active and has started transmitting a Mark-1 on the Lines. The protocol waits for a time T_{wakeup} and then drives TxRequestEsc (TxUlpsClk) inactive to return the Lane to Stop state.</p> <p>For a receiver, this signal indicates that the Lane is in ULP state. When entering the ULP state, RxUlpsEsc (or RxUlpsClkNot for a Clock Lane) is asserted to indicate the detection of the ULPS command and entry into the ULP state, followed by the assertion of the UlpsActiveNot, indicating that the PHY is in the ULP state. When exiting the ULP</p>
continued...			

Signal	Direction	Width	Description
			state, this signal is deasserted to indicate that the PHY has detected a Mark-1 to initiate the exit from the ULP state. After the required TWAKEUP, the RxUlpsEsc, or RxUlpsClkNot for a Clock Lane, is deasserted to indicate the PHY has exited the ULP state and LP-11 has been detected.
LINKn_Dm_TxHSIdleClkHS	Input	1	HS-Idle State Start (link n, data lane m).
LINKn_Dm_TxHSIdleClkReadyHS	Output	1	Clock Ready to Exit HS-Idle-ClkHS0 Sub-State (link n, data lane m).
Error Signals (Link n, Data Lane m)			
LINKn_Dm_ErrSotHS	Output	1	Start-of-Transmission (SoT) Error (link n, data lane m) If the High-Speed SoT leader sequence is corrupted, but in such a way that proper synchronization can still be achieved, this active high signal is asserted for one cycle of RxWordClkHS. This is considered to be a "soft error" in the leader sequence and confidence in the payload data is reduced. When there is a Start-of-Transmission (SoT) Error, ErrSotHS is asserted in the same cycle as RxSyncHS is asserted.
LINKn_Dm_ErrSotSyncHS	Output	1	Start-of-Transmission Synchronization Error (link n, data lane m) If the High-Speed SoT leader sequence is corrupted in a way that proper synchronization cannot be expected, this active high signal is asserted for one cycle of RxWordClkHS. When ErrSotSyncHS is asserted, RxSyncHS, ErrSotHS, and RxValidHS is not asserted.
LINKn_Dm_ErrEsc	Output	1	Escape Entry Error (link n, data lane m) If an unrecognized escape entry command is received in LP mode, this active high signal is asserted and remains asserted until the next transaction starts, so that the protocol can properly process the error.
LINKn_Dm_ErrSyncEsc	Output	1	Low-Power Data Transmission Synchronization Error (link n, data lane m) If the number of bits received during a LP data transmission is not a multiple of eight when the transmission ends, this active high signal is asserted and remains asserted until the next transaction starts, so that the protocol can properly process the error.
LINKn_Dm_ErrControl	Output	1	Control Error (link n, data lane m) This active-high signal is asserted when an incorrect Line state sequence is detected in LP and ALP modes. Once asserted, this signal remains asserted until the next transaction starts, so that the protocol can properly process the error. Section A.18 describes the LP and ALP signaling error sequences that require this signal to be asserted, as well as error sequences that can optionally result in this signal being asserted. Sequences that can optionally result in this signal being asserted are implementation specific.
LINKn_Dm_ErrContentionLP0	Output	1	LP0 Contention Error (link n, data lane m).
LINKn_Dm_ErrContentionLP1	Output	1	LP1 Contention Error (link n, data lane m).

8.1.5. D-PHY TX PPI Interface Signals

These PPI interface signals are available when the D-PHY IP is configured for transmit. Each lane (clock and data) of each link has a TX PPI interface attached to it.

Figure 25. PPI Interface Signals (Clock and Data Lanes)

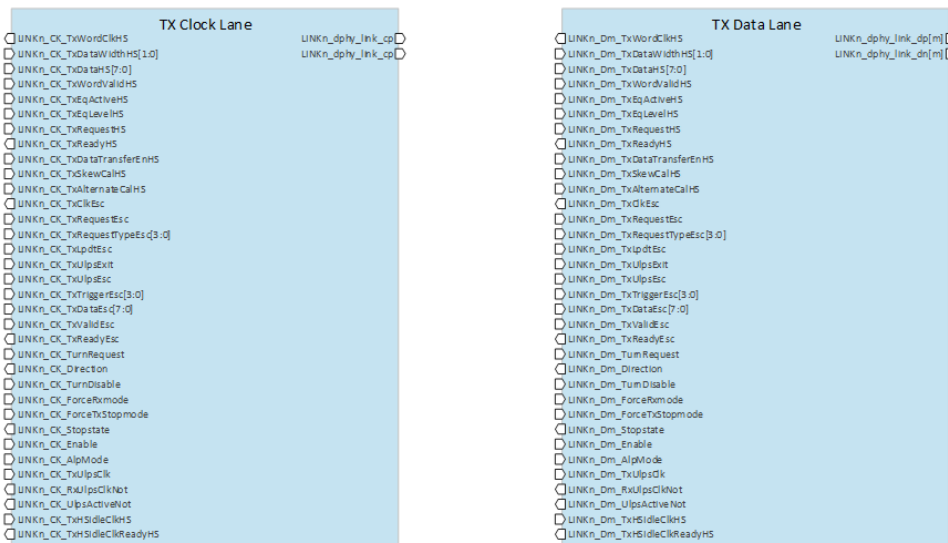


Table 24. PPI TX Interface - Link n, Clock Lane

Signal	Direction	Width	Description
High-Speed Transmit Signals (Link n, Clock Lane) - TX only			
LINKn_CK_TxWordClkHS	Output	1	High-Speed Transmit Word Clock (link n, clock lane) This is used to synchronize PPI signals in the high-speed transmit clock domain. It is recommended that all transmitting Lane Modules share one TxWordClkHS signal. The frequency of TxWordClkHS is dependent upon the width of the High-Speed Transmit Data, as follows: • 16-bit width, TxDataHS[15:0], the High-Speed Transmit Word Clock is exactly 1/16 the high-speed data rate.
LINKn_CK_TxDataWidthHS	Input	2	High-Speed Transmit Data bus Width Select (link n, clock lane).
LINKn_CK_TxDataHS	Input	8	High-Speed Transmit Data bus (link n, clock lane).
LINKn_CK_TxWordValidHS	Input	1	High-Speed Transmit Word Data Valid (link n, clock lane) When the High-Speed Transmit Data width is greater than 8 bits it is necessary to indicate which 8-bit segments contain valid transmit data to be able to transmit any number of words. The following TxWordValidHS signals are defined based on the width of the transmit data path: • 16-bit width – TxWordValidHS[1:0] The following Transmit Word Data Valid signals indicate which bits of the TxDataHS data bus contain valid data to transmit as follows: • TxWordValidHS[0] – TxDataHS[7:0] contains valid data to be transmitted • TxWordValidHS[1] – TxDataHS[15:8] contains valid data to be transmitted For a 16-bit transmit data width with multiple words being transferred, TxWordValidHS[1:0] is driven to 0x3 on the first word of the data transfer and either 0x1 or 0x3 on the last word of the
<i>continued...</i>			

Signal	Direction	Width	Description
			data transfer. If there are more than 2 words transferred, TxWordValidHS[1:0] is driven to 0x3 for all of the middle word data transfers. If only one word is being transferred, TxWordValidHS[1:0] is driven to either 0x1 or 0x3.
LINKn_CK_TxEqActiveHS	Input	1	High-Speed Transmit Equalization Enable (link n, clock lane).
LINKn_CK_TxEqLevelHS	Input	1	High-Speed Transmit Equalization Level (link n, clock lane).
LINKn_CK_TxRequestHS	Input	1	High-Speed Transmit Request and Data Valid (link n, clock lane) A low-to-high transition on TxRequestHS causes the Lane Module to initiate a Start-of-Transmission sequence. A high-to-low transition on TxRequest causes the Lane Module to initiate an End-of-Transmission sequence. For Clock Lanes, this active high signal causes the Lane Module to begin transmitting a High-Speed clock. For Data Lanes, this active high signal also indicates that the protocol is driving valid data on TxDataHS to be transmitted. The Lane Module accepts the data when both TxRequestHS and TxReadyHS are active on the same rising TxWordClkHS clock edge. The protocol always provides valid transmit data when TxRequestHS is active. Once asserted, TxRequestHS remains high until the data has been accepted, as indicated by TxReadyHS. TxRequestHS is only asserted while TxRequestEsc is low. A low-to-high transition on TxRequestHS can only happen when Stopstate is asserted. The protocol layer asserts TxRequestHS for the clock Lane at the same clock cycle or in previous clock cycles of the TxRequestHS of the data Lanes. The protocol layer asserts TxRequestHS for the clock Lane for every cycle that TxRequestHS is asserted for the data Lanes. The PHY guarantees TCLK-PRE and TCLK-POST timing parameters. The TxRequestHS for clock Lane will be kept asserted after the TxRequestHS for data Lanes have been deasserted, for cases of applications where continued availability of the clock is necessary. The assertion of this signal is mutually exclusive with the assertion of the TxSkewCalHS, TxAlternateCalHS, and TxRequestEsc signals.
LINKn_CK_TxReadyHS	Output	1	High-Speed Transmit Ready (link n, clock lane) For clock Lanes, this active high signal indicates that the Lane is currently transmitting a High-Speed clock. For data Lanes, this active high signal indicates that TxDataHS is accepted by the Lane Module to be serially transmitted. TxReadyHS is valid on rising edges of TxWordClkHS. Optionally, TxReadyHS can be used during deskew calibration to indicate that SoT has ended and data Lanes are transmitting deskew burst (clock pattern).
LINKn_CK_TxDataTransferEnHS	Input	1	High-Speed Tx Data Transfer Enable (link n, clock lane).
LINKn_CK_TxSkewCalHS	Input	1	High-Speed Transmit Skew Calibration (link n, clock lane).
LINKn_CK_TxAlternateCalHS	Input	1	High-Speed Transmit Alternate Calibration (link n, clock lane).
Escape Mode Transmit Signals (Link n, Clock Lane) - TX only			
LINKn_CK_TxCkEsc	Output	1	Escape Mode Transmit Clock (link n, clock lane) This clock is directly used to time escape sequences on the PPI. For LP mode, the period of this clock determines the phase times for Low-Power signals as defined in Section 6.6.2. It is therefore constrained by the normative part of the D-PHY specification. See Section 9 Note that the TurnRequest signal is synchronous to this clock and this clock is included for any module that supports Bi-directional High-Speed operation, even if that module does not support transmit or Bi-directional Escape Mode. For ALP mode, this clock is not

continued...

Signal	Direction	Width	Description
			used to time the signaling on the serial line. Although not required, gains in efficiency of a given implementation can be achieved by requiring this clock to be phase and frequency aligned with the TxWordClkHS clock.
LINKn_CK_TxRequestEsc	Input	1	Escape Mode Transmit Request (link n, clock lane).
LINKn_CK_TxRequestTypeEsc	Input	4	Escape Mode Transmit Request Type (link n, clock lane).
LINKn_CK_TxLpdtEsc	Input	1	Escape Mode Transmit Low-Power Data (link n, clock lane).
LINKn_CK_TxUlpsExit	Input	1	Transmit ULP Exit Sequence (link n, clock lane) This active high signal is asserted when ULP state is active and the protocol is ready to leave ULP state. The PHY leaves ULP state and begins driving Mark-1 after TxUlpsExit is asserted. The PHY later drives the Stop state (LP-11) when TxRequestEsc is deasserted. TxUlpsExit is synchronous to TxClkEsc. This signal is ignored when the Lane is not in the ULP State.
LINKn_CK_TxUlpsEsc	Input	1	Escape Mode Transmit Ultra-Low Power State (link n, clock lane) For LP implementations, this active high signal is asserted with TxRequestEsc to cause the Lane Module to enter the Ultra-Low Power State. The Lane Module remains in this mode until TxRequestEsc is de-asserted. TxLpdtEsc and all bits of TxTriggerEsc are low when TxUlpsEsc is asserted. For ALP implementations, this signal is unused and if present, must be driven low during ALP requests.
LINKn_CK_TxTriggerEsc	Input	4	Escape Mode Transmit Trigger 0-3 (link n, clock lane) .
LINKn_CK_TxDataEsc	Input	8	Escape Mode Transmit Data (link n, clock lane).
LINKn_CK_TxValidEsc	Input	1	Escape Mode Transmit Data Valid (link n, clock lane).
LINKn_CK_TxReadyEsc	Output	1	Escape Mode Transmit Ready (link n, clock lane).
Control Signals (Link n, Clock Lane)			
LINKn_CK_TurnRequest	Input	1	Turnaround Request (link n, clock lane).
LINKn_CK_Direction	C	1	Transmit/Receive Direction (link n, clock lane) This signal is used to indicate the current direction of the Lane interconnect. When Direction=0, the Lane is in transmit mode (0=Output). When Direction=1, the Lane is in receive mode (1=Input). When transitioning from TX to RX, the direction changes state after completion of a successful BTA procedure, as indicated by the detection of Mark-1 followed by LP-11. When transitioning from RX to TX, the direction changes state after the TTA-SURE time has been met, and the local driver starts transmitting LP-00. Any abnormalities during the BTA procedure can result in contention conditions, requiring the protocol layer to implement mechanisms to detect and resolve.
LINKn_CK_TurnDisable	Input	1	Disable Turnaround (link n, clock lane).
LINKn_CK_ForceRxmode	Input	1	Force Lane Module Into Receive mode / Wait for Stop state (link n, clock lane) - RX only This signal allows the protocol to initialize a Lane Module, or force a Bi-directional Lane Module, into receive mode. This signal is used during initialization or to resolve a contention situation. When this signal is high, the Lane Module immediately transitions into receive Control mode and waits for a Stop state to appear on the Lane interconnect. When used for initialization, this signal will be released (i.e., driven low) only when the Dp Dn inputs are in Stop state for a time TINIT, or longer. The assertion of ForceRxmode and ForceTxStopmode are mutually exclusive.
continued...			

Signal	Direction	Width	Description
LINKn_CK_ForceTxStopmode	Input	1	Force Lane Module Into Transmit mode / Generate Stop state (link n, clock lane) - TX only This signal allows the protocol to force a Lane Module into transmit mode and Stop state during initialization or following an error situation, e.g. expired time out. When this signal is high, the Lane Module immediately transitions into transmit mode and the module state machine is forced into the Stop state. The protocol layer does not assert TxRequestEsc, TxRequestHS, or Turnrequest for an implementation-specific period of time after the deassertion of ForceTxStopMode, in order to create a safe margin for the PHY to be able to accept a new request. The assertion of ForceRxmode and ForceTxStopmode are mutually exclusive.
LINKn_CK_Stopstate	Output	1	Lane is in Stop state (link n, clock lane) This active high signal indicates that the Lane Module, regardless of whether the Lane Module is a transmitter or a receiver, is currently in Stop state. This indicates that the PHY Line levels are in the LP-11 state, and the PHY state machine is in the stop state and ready to receive a request for the next operation. Also, the protocol may use this signal to indirectly determine if the PHY Line levels are in the LP-11 state. A Master will not assert this signal during initialization until after LP-11 has been driven for the required T _{INIT} time. A Slave will not assert this signal during initialization until after LP-11 has been detected for the required T _{INIT} time.
LINKn_CK_Enable	Input	1	Enable Lane Module (link n, clock lane) This active high signal forces the Lane Module out of "shutdown". All Line drivers, receivers, terminators, and contention detectors are turned off when Enable is low. Furthermore, while Enable is low, all other PPI inputs are ignored, and all PPI outputs are driven to the default inactive state. Enable is a level sensitive signal and does not depend on any clock.
LINKn_CK_AlpMode	Input	1	Alternate Low Power Mode Selection (link n, clock lane).
LINKn_CK_TxUlpsClk	Input	1	Transmit Ultra-Low Power State on Clock Lane (link n, clock lane) - TX only This active high signal is asserted to cause a Clock Lane Module to enter the Ultra-Low Power State. The Lane Module remains in this mode until TxUlpsClk is de-asserted.
LINKn_CK_RxUlpsClkNot	Output	1	Receive Ultra-Low Power State on Clock Lane (link n, clock lane) - RX only This active low signal is asserted to indicate that the Clock Lane Module has entered the Ultra-Low Power State due to the detection of a request to enter the ULP state. The Lane Module remains in this mode with RxUlpsClkNot asserted until a Stop state is detected on the Lane Interconnect.
LINKn_CK_UlpsActiveNot	Output	1	ULP State (not) Active (link n, clock lane) This active low signal is asserted to indicate that the Lane is in ULP state. For a transmitter, this signal is asserted some time after TxUlpsEsc and TxRequestEsc (TxUlpsClk for a Clock Lane) are asserted. The transmitting PHY continues to supply TxClkEsc until UlpsActiveNot is asserted. In order to leave ULP state, the transmitter first drives TxUlpsExit high, then waits for UlpsActiveNot to become high (inactive). At that point, the transmitting PHY is active and has started transmitting a Mark-1 on the Lines. The protocol waits for a time Twakeup and then drives TxRequestEsc (TxUlpsClk) inactive to return the Lane to Stop state. For a receiver, this signal indicates that the Lane is in ULP state. When entering the ULP state, RxUlpsEsc (or RxUlpsClkNot for a Clock Lane) is asserted to indicate the detection of the ULPS command and entry into the ULP state, followed by the assertion of the UlpsActiveNot, indicating that the PHY is in the ULP

continued...

Signal	Direction	Width	Description
			state. When exiting the ULP state, this signal is deasserted to indicate that the PHY has detected a Mark-1 to initiate the exit from the ULP state. After the required TWAKEUP, the RxUlpsEsc, or RxUlpsClkNot for a Clock Lane, is deasserted to indicate the PHY has exited the ULP state and LP-11 has been detected.
LINKn_CK_TxHSIdleClkHS	Input	1	HS-Idle State Start (link n, clock lane).
LINKn_CK_TxHSIdleClkReadyHS	Output	1	Clock Ready to Exit HS-Idle-ClkHS0 Sub-State (link n, clock lane).

Table 25. PPI TX Interface - Link *n*, Data Lane *m*

Signal	Direction	Width	Description
High-Speed Transmit Signals (Link <i>n</i>, Data Lane <i>m</i>) - TX only			
LINKn_Dm_TxWordClkHS	Output	1	High-Speed Transmit Word Clock (link <i>n</i> , data lane <i>m</i>) This is used to synchronize PPI signals in the high-speed transmit clock domain. It is recommended that all transmitting Lane Modules share one TxWordClkHS signal. The frequency of TxWordClkHS is dependent upon the width of the High-Speed Transmit Data, as follows: • 16-bit width, TxDataHS[15:0], the High-Speed Transmit Word Clock is exactly 1/16 the high-speed data rate.
LINKn_Dm_TxDataWidthHS	Input	2	High-Speed Transmit Data bus Width Select (link <i>n</i> , data lane <i>m</i>) Selects the bus width of TxDataHS: • TxDataWidthHS[1:0] = 00: not used, reserved. • TxDataWidthHS[1:0] = 01: 16-bit, TxDataHS[15:0] • TxDataWidthHS[1:0] = 10: not used, reserved • TxDataWidthHS[1:0] = 11: not used, reserved. An implementation may support any data width - one fixed width, or subset of widths or all widths defined above.
LINKn_Dm_TxDataHS	Input	8	High-Speed Transmit Data bus (link <i>n</i> , data lane <i>m</i>) High-speed data to be transmitted. If the TxWordValidHS signals indicate that more than 8 bits are to be transmitted, then the byte transmission order over the physical interface is TxDataHS[7:0] followed by TxDataHS[15:8]. Data is captured on rising edges of TxWordClkHS. The following signals are defined for the High-Speed Transmit Data bus based on the width of the transmit data path: • 16-bit width - TxDataHS[15:0] An implementation may support any data width - one fixed width, or subset of widths or all widths defined above. The LSB will be transmitted as the first bit and the MSB will be transmitted as the last bit.
LINKn_Dm_TxWordValidHS	Input	1	High-Speed Transmit Word Data Valid (link <i>n</i> , data lane <i>m</i>) When the High-Speed Transmit Data width is greater than 8 bits it is necessary to indicate which 8-bit segments contain valid transmit data to be able to transmit any number of words. The following TxWordValidHS signals are defined based on the width of the transmit data path: • 16-bit width - TxWordValidHS[1:0] The following Transmit Word Data Valid signals indicate which bits of the TxDataHS data bus contain valid data to transmit as follows: • TxWordValidHS[0] -
continued...			

Signal	Direction	Width	Description
			TxDataHS[7:0] contains valid data to be transmitted • TxWordValidHS[1] – TxDataHS[15:8] contains valid data to be transmitted For a 16-bit transmit data width with multiple words being transferred, TxWordValidHS[1:0] is driven to 0x3 on the first word of the data transfer and either 0x1 or 0x3 on the last word of the data transfer. If there are more than 2 words transferred, TxWordValidHS[1:0] is driven to 0x3 for all of the middle word data transfers. If only one word is being transferred, TxWordValidHS[1:0] is driven to either 0x1 or 0x3.
LINKn_Dm_TxEqActiveHS	Input	1	High-Speed Transmit Equalization Enable (link n, data lane m).
LINKn_Dm_TxEqLevelHS	Input	1	High-Speed Transmit Equalization Level (link n, data lane m).
LINKn_Dm_TxRequestHS	Input	1	High-Speed Transmit Request and Data Valid (link n, data lane m) A low-to-high transition on TxRequestHS causes the Lane Module to initiate a Start-of-Transmission sequence. A high-to-low transition on TxRequest causes the Lane Module to initiate an End-of-Transmission sequence. For Clock Lanes, this active high signal causes the Lane Module to begin transmitting a High-Speed clock. For Data Lanes, this active high signal also indicates that the protocol is driving valid data on TxDataHS to be transmitted. The Lane Module accepts the data when both TxRequestHS and TxReadyHS are active on the same rising TxWordClkHS clock edge. The protocol always provides valid transmit data when TxRequestHS is active. Once asserted, TxRequestHS remains high until the data has been accepted, as indicated by TxReadyHS. TxRequestHS is only asserted while TxRequestEsc is low. A low-to-high transition on TxRequestHS can only happen when Stopstate is asserted. The protocol layer asserts TxRequestHS for the clock Lane at the same clock cycle or in previous clock cycles of the TxRequestHS of the data Lanes. The protocol layer asserts TxRequestHS for the clock Lane for every cycle that TxRequestHS is asserted for the data Lanes. The PHY guarantees TCLK-PRE and TCLK-POST timing parameters. The TxRequestHS for clock Lane will be kept asserted after the TxRequestHS for data Lanes have been deasserted, for cases of applications where continued availability of the clock is necessary. The assertion of this signal is mutually exclusive with the assertion of the TxSkewCalHS, TxAlternateCalHS, and TxRequestEsc signals.
LINKn_Dm_TxReadyHS	Output	1	High-Speed Transmit Ready (link n, data lane m) For clock Lanes, this active high signal indicates that the Lane is currently transmitting a High-Speed clock. For data Lanes, this active high signal indicates that TxDataHS is accepted by the Lane Module to be serially transmitted. TxReadyHS is valid on rising edges of TxWordClkHS. Optionally, TxReadyHS can be used during deskew calibration to indicate that SoT has ended and data Lanes are transmitting deskew burst (clock pattern).
continued...			

Signal	Direction	Width	Description
LINKn_Dm_TxDataTransferEnHS	Input	1	High-Speed Tx Data Transfer Enable (link n, data lane m) This active high signal that is synchronous to TxWordClkHS indicates to the PHY that TxDataHS is valid. When this signal is deasserted and Preamble is disabled, the PHY must remain in the HS-Zero State even if TxReadyHS is asserted. If Preamble is enabled, the PHY must remain in the Preamble state even if TxReadyHS is asserted until TxDataTransferEnHS is asserted. Once asserted, the protocol layer can only deassert this signal when TxRequestHS is also deasserted. TxDataTransferEnHS can be tied high, if the protocol layer does not support High Speed Tx Data Transfer Enable, or if it does not want to throttle TxDataHS at the beginning of a HS data transfer.
LINKn_Dm_TxSkewCalHS	Input	1	High-Speed Transmit Skew Calibration (link n, data lane m) This is an optional signal to initiate the periodic deskew burst at the transmitter. A low-to-high transition on TxSkewCalHS causes the PHY to initiate the transmission of a skew calibration pattern. A high-to-low transition on TxSkewCalHS causes the PHY to end the transmission of a skew calibration pattern, and initiate an end-of-transmission sequence. Note that TxSkewCalHS is used to generate both the initial and periodic skew calibration patterns. The assertion of this signal is mutually exclusive with the assertion of the TxRequestHS, TxAlternateCalHS, and TxRequestEsc signals. When TxSkewCalHS is asserted, TxRequestHS will be asserted on the clock Lane. All data Lanes for a Link can initiate the deskew pattern at the same time.
LINKn_Dm_TxAlternateCalHS	Input	1	High-Speed Transmit Alternate Calibration (link n, data lane m) This is an optional signal to initiate the alternate calibration sequence at the transmitter. A low-to-high transition on TxAlternateCalHS causes the PHY to initiate an alternate calibration sequence. A high-to-low transition on TxAlternateCalHS causes the PHY to stop the alternate calibration sequence and initiate an end-of-transmission sequence. The assertion of this signal is mutually exclusive with the assertion of the TxRequestHS, TxSkewCalHS, and TxRequestEsc signals. When TxAlternateCalHS is asserted, TxRequestHS will be asserted on the clock Lane. All data Lanes for a Link can initiate alternate calibration sequence at the same time. It is up to the protocol layer to ensure TxAlternateCalHS is only asserted after the initial deskew pattern and before any High Speed data transfers.
Escape Mode Transmit Signals (Link n, Data Lane m) - TX only			
LINKn_Dm_TxClockEsc	Output	1	Escape Mode Transmit Clock (link n, data lane m) This clock is directly used to time escape sequences on the PPI. For LP mode, the period of this clock determines the phase times for Low-Power signals as defined in Section 6.6.2. It is therefore constrained by the normative part of the D-PHY specification. See Section 9 Note that the TurnRequest signal is synchronous to this clock and this clock is included for any module that supports Bi-directional High-Speed operation, even if that module does not support transmit or Bi-directional
<i>continued...</i>			

Signal	Direction	Width	Description
			Escape Mode. For ALP mode, this clock is not used to time the signaling on the serial line. Although not required, gains in efficiency of a given implementation can be achieved by requiring this clock to be phase and frequency aligned with the TxWordClkHS clock.
LINKn_Dm_TxRequestEsc	Input	1	Escape Mode Transmit Request (link n, data lane m) This active high signal is used to request escape sequences. Once an escape sequence starts, the Lane continues driving the escape sequence until TxRequestEsc is de-asserted. For LP implementations, this signal is asserted together with exactly one of TxLpdtEsc, TxUlpsEsc, or one bit of TxTriggerEsc, or alternatively the TxRequestTypeEsc. For ALP implementations, this signal is asserted together with TxRequestTypeEsc. The requirements for the deassertion of TxRequestEsc are as follows: <ul style="list-style-type: none"> • When transmitting low power data, TxRequestEsc is deasserted after TxReadyEsc is asserted for the final byte of data. • When requesting ULPS entry, TxRequestEsc is deasserted Twakeup time after UlpsActiveNot is deasserted in response to TxUlpsExit being asserted. • When transmitting a trigger, TxRequestEsc is deasserted at any time after the request is made. If the PHY has not completed the transmission of the trigger command at the time that TxRequestEsc is deasserted, the PHY will complete the transmission then drive Mark-1 and LP-11. If the PHY has completed the transmission of the trigger command and TxRequestEsc is not deasserted, the PHY will transmit either the required space state, or the optional dummy data bytes in order to generate clocks on RxClkEsc of the receiver until TxRequestEsc is deasserted, at which time the PHY will complete the current transmission then drive Mark-1 and LP-11. The assertion of this signal is mutually exclusive with the assertion of the TxRequestHS, TxSkewCalHS, and TxAlternateCalHS signals. A low-to-high transition on TxRequestEsc can only happen when Stopstate is asserted.
LINKn_Dm_TxRequestTypeEsc	Input	4	Escape Mode Transmit Request Type (link n, data lane m) This signal is required for ALP implementations and optional for LP implementations. When implemented with LP implementations, it can be used in place of the TxLpdtEsc, TxUlpsEsc, and TxTriggerEsc signals. This signal indicates the type of transmit that is being requested. It is driven at the same time as TxRequestEsc and remains active until Stopstate is asserted. The encoding of this signal is as follows: <ul style="list-style-type: none"> • 0000: Reserved (do not use) • 0001: Ultra low power state (ULPS) • 0010: Undefined-1 • 0011: Undefined-2 • 0100: Trigger 0 - Reset trigger • 0101: Trigger 1 - Entry sequence for HS Test mode • 0110: Trigger 2 • 0111: Trigger 3 • 1000: Reserved • 1001: Reserved • 1010: Wakeup pulse (not for initiating ULPS exit) • 1011 - 1111: Reserved.
LINKn_Dm_TxLpdtEsc	Input	1	Escape Mode Transmit Low-Power Data (link n, data lane m) For LP implementations, this active high signal is asserted with TxRequestEsc to cause the Lane Module to enter Low-Power data transmission mode. The Lane Module remains in

continued...

Signal	Direction	Width	Description
			this mode until TxRequestEsc is de-asserted. TxUlpsEsc and all bits of TxTriggerEsc are low when TxLpdtEsc is asserted. For ALP implementations, this signal is unused and if present, must be driven low during ALP requests.
LINKn_Dm_TxUlpsExit	Input	1	Transmit ULP Exit Sequence (link n, data lane m) This active high signal is asserted when ULP state is active and the protocol is ready to leave ULP state. The PHY leaves ULP state and begins driving Mark-1 after TxUlpsExit is asserted. The PHY later drives the Stop state (LP-11) when TxRequestEsc is deasserted. TxUlpsExit is synchronous to TxClkEsc. This signal is ignored when the Lane is not in the ULP State.
LINKn_Dm_TxUlpsEsc	Input	1	Escape Mode Transmit Ultra-Low Power State (link n, data lane m) For LP implementations, this active high signal is asserted with TxRequestEsc to cause the Lane Module to enter the Ultra-Low Power State. The Lane Module remains in this mode until TxRequestEsc is de-asserted. TxLpdtEsc and all bits of TxTriggerEsc are low when TxUlpsEsc is asserted. For ALP implementations, this signal is unused and if present, must be driven low during ALP requests.
LINKn_Dm_TxTriggerEsc	Input	4	Escape Mode Transmit Trigger 0-3 (link n, data lane m) For LP implementations, one of these active high signals is asserted with TxRequestEsc to cause the associated Trigger to be sent across the Lane interconnect. In the receiving Lane Module, the same bit of RxTriggerEsc is then asserted and remains asserted until the Lane interconnect returns to Stop state, which happens when TxRequestEsc is de-asserted at the transmitter. Only one bit of TxTriggerEsc is asserted at any given time, and only when TxLpdtEsc and TxUlpsEsc are both low. TxTriggerEsc[0] corresponds to Reset-Trigger. TxTriggerEsc[1] corresponds to Entry sequence for HS Test mode Trigger. TxTriggerEsc[2] corresponds to Unknown-4 Trigger. TxTriggerEsc[3] corresponds to Unknown-5 Trigger. For ALP implementations, this signal is unused and if present, must be driven low during ALP requests.
LINKn_Dm_TxDataEsc	Input	8	Escape Mode Transmit Data (link n, data lane m) - Data lane 0 only This is the eight bit Escape Mode data to be transmitted in Low-Power data transmission mode. The signal connected to TxDataEsc[0] is transmitted first. Data is captured on rising edges of TxClkEsc.
LINKn_Dm_TxValidEsc	Input	1	Escape Mode Transmit Data Valid (link n, data lane m) - Data lane 0 only This active high signal indicates that the protocol is driving valid data on TxDataEsc to be transmitted. The Lane Module accepts the data when TxRequestEsc, TxValidEsc and TxReadyEsc are all active on the same rising TxClkEsc clock edge.
LINKn_Dm_TxReadyEsc	Output	1	Escape Mode Transmit Ready (link n, data lane m) - Data lane 0 only This active high signal indicates that TxDataEsc is accepted by the Lane Module to be serially transmitted. TxReadyEsc is valid on rising edges of TxClkEsc.
continued...			

Signal	Direction	Width	Description
Control Signals (Link <i>n</i>, Data Lane <i>m</i>)			
LINKn_Dm_TurnRequest	Input	1	Turnaround Request (link <i>n</i> , data lane <i>m</i>).
LINKn_Dm_Direction	Output	1	Transmit/Receive Direction (link <i>n</i> , data lane <i>m</i>) This signal is used to indicate the current direction of the Lane interconnect. When Direction=0, the Lane is in transmit mode (0=Output). When Direction=1, the Lane is in receive mode (1=Input). When transitioning from TX to RX, the direction changes state after completion of a successful BTA procedure, as indicated by the detection of Mark-1 followed by LP-11. When transitioning from RX to TX, the direction changes state after the TTA-SURE time has been met, and the local driver starts transmitting LP-00. Any abnormalities during the BTA procedure can result in contention conditions, requiring the protocol layer to implement mechanisms to detect and resolve.
LINKn_Dm_TurnDisable	Input	1	Disable Turnaround (link <i>n</i> , data lane <i>m</i>).
LINKn_Dm_ForceRxmode	Input	1	Force Lane Module Into Receive mode / Wait for Stop state (link <i>n</i> , data lane <i>m</i>) - RX only This signal allows the protocol to initialize a Lane Module, or force a Bi-directional Lane Module, into receive mode. This signal is used during initialization or to resolve a contention situation. When this signal is high, the Lane Module immediately transitions into receive Control mode and waits for a Stop state to appear on the Lane interconnect. When used for initialization, this signal will be released (i.e., driven low) only when the Dp Dn inputs are in Stop state for a time T _{INIT} , or longer. The assertion of ForceRxmode and ForceTxStopmode are mutually exclusive.
LINKn_Dm_ForceTxStopmode	Input	1	Force Lane Module Into Transmit mode / Generate Stop state (link <i>n</i> , data lane <i>m</i>) - TX only This signal allows the protocol to force a Lane Module into transmit mode and Stop state during initialization or following an error situation, e.g. expired time out. When this signal is high, the Lane Module immediately transitions into transmit mode and the module state machine is forced into the Stop state. The protocol layer does not assert TxRequestEsc, TxRequestHS, or Turnrequest for an implementation-specific period of time after the deassertion of ForceTxStopMode, in order to create a safe margin for the PHY to be able to accept a new request. The assertion of ForceRxmode and ForceTxStopmode are mutually exclusive.
LINKn_Dm_Stopstate	Output	1	Lane is in Stop state (link <i>n</i> , data lane <i>m</i>) This active high signal indicates that the Lane Module, regardless of whether the Lane Module is a transmitter or a receiver, is currently in Stop state. This indicates that the PHY Line levels are in the LP-11 state, and the PHY state machine is in the stop state and ready to receive a request for the next operation. Also, the protocol may use this signal to indirectly determine if the PHY Line levels are in the LP-11 state. A Master will not assert this signal during initialization until after LP-11 has been driven for the required T _{INIT} time. A Slave will
continued...			

Signal	Direction	Width	Description
			not assert this signal during initialization until after LP-11 has been detected for the required T_{INIT} time.
LINKn_Dm_Enable	Input	1	Enable Lane Module (link n, data lane m) This active high signal forces the Lane Module out of "shutdown". All Line drivers, receivers, terminators, and contention detectors are turned off when Enable is low. Furthermore, while Enable is low, all other PPI inputs are ignored, and all PPI outputs are driven to the default inactive state. Enable is a level sensitive signal and does not depend on any clock.
LINKn_Dm_AlpMode	Input	1	Alternate Low Power Mode Selection (link n, data lane m).
LINKn_Dm_TxUlpsClk	Input	1	Transmit Ultra-Low Power State on Clock Lane (link n, data lane m) - TX only This active high signal is asserted to cause a Clock Lane Module to enter the Ultra-Low Power State. The Lane Module remains in this mode until TxUlpsClk is de-asserted.
LINKn_Dm_RxUlpsClkNot	Output	1	Receive Ultra-Low Power State on Clock Lane (link n, data lane m) - RX only This active low signal is asserted to indicate that the Clock Lane Module has entered the Ultra-Low Power State due to the detection of a request to enter the ULP state. The Lane Module remains in this mode with RxUlpsClkNot asserted until a Stop state is detected on the Lane Interconnect.
LINKn_Dm_UlpsActiveNot	Output	1	ULP State (not) Active (link n, data lane m) This active low signal is asserted to indicate that the Lane is in ULP state. For a transmitter, this signal is asserted some time after TxUlpsEsc and TxRequestEsc (TxUlpsClk for a Clock Lane) are asserted. The transmitting PHY continues to supply TxClkEsc until UlpsActiveNot is asserted. In order to leave ULP state, the transmitter first drives TxUlpsExit high, then waits for UlpsActiveNot to become high (inactive). At that point, the transmitting PHY is active and has started transmitting a Mark-1 on the Lines. The protocol waits for a time Twakeup and then drives TxRequestEsc (TxUlpsClk) inactive to return the Lane to Stop state. For a receiver, this signal indicates that the Lane is in ULP state. When entering the ULP state, RxUlpsEsc (or RxUlpsClkNot for a Clock Lane) is asserted to indicate the detection of the ULPS command and entry into the ULP state, followed by the assertion of the UlpsActiveNot, indicating that the PHY is in the ULP state. When exiting the ULP state, this signal is deasserted to indicate that the PHY has detected a Mark-1 to initiate the exit from the ULP state. After the required TWAKEUP, the RxUlpsEsc, or RxUlpsClkNot for a Clock Lane, is deasserted to indicate the PHY has exited the ULP state and LP-11 has been detected.
LINKn_Dm_TxHSIdleClkHS	Input	1	HS-Idle State Start (link n, data lane m).
LINKn_Dm_TxHSIdleClkReadyHS	Output	1	Clock Ready to Exit HS-Idle-ClkHS0 Sub-State (link n, data lane m).

8.1.6. AXI-Lite CSR Access

The D-PHY IP has a single AXI-Lite bus that allows the protocol agent in the fabric to access the CSR of the D-PHY.

Multiple links are accessed from the same AXI-Lite interface using the memory map described below. Aside from allowing access to the D-PHY internal IP registers, the AXI-Lite bus is designed to allow access to external registers which are used for accessing the PPI TG.

Table 26. D-PHY IP Register Map

Start	End	Link Number	Register Space
0x000	0x07F	0	D-PHY IP registers for Link 0
0x080	0x0FF		D-PHY IP shared (mirrored)
0x100	0x17F		External Shared (mirrored)
0x180	0x1FF		External registers for Link 0
0x200	0x27F	1	D-PHY IP registers for Link 1
0x280	0x2FF		D-PHY IP shared (mirrored)
0x300	0x37F		External Shared (mirrored)
0x380	0x3FF		External registers for Link 1
0x400	0x47F	2	D-PHY IP registers for Link 2
0x480	0x4FF		D-PHY IP shared (mirrored)
0x500	0x57F		External Shared (mirrored)
0x580	0x5FF		External registers for Link 2
0x600	0x67F	3	D-PHY IP registers for Link 3
0x680	0x6FF		D-PHY IP shared (mirrored)
0x700	0x77F		External Shared (mirrored)
0x780	0x7FF		External registers for Link 3
0x800	0x87F	4	D-PHY IP registers for Link 4
0x880	0x8FF		D-PHY IP shared (mirrored)
0x900	0x97F		External Shared (mirrored)
0x980	0x9FF		External registers for Link 4
0xA00	0xA7F	5	D-PHY IP registers for Link 5
0xA80	0xAFF		D-PHY IP shared (mirrored)
0xB00	0xB7F		External Shared (mirrored)
0xB80	0xBFF		External registers for Link 5
0xC00	0xC7F	6	D-PHY IP registers for Link 6
0xC80	0xCFF		D-PHY IP shared (mirrored)
0xD00	0xD7F		External Shared (mirrored)
0xD80	0xDFF		External registers for Link 6

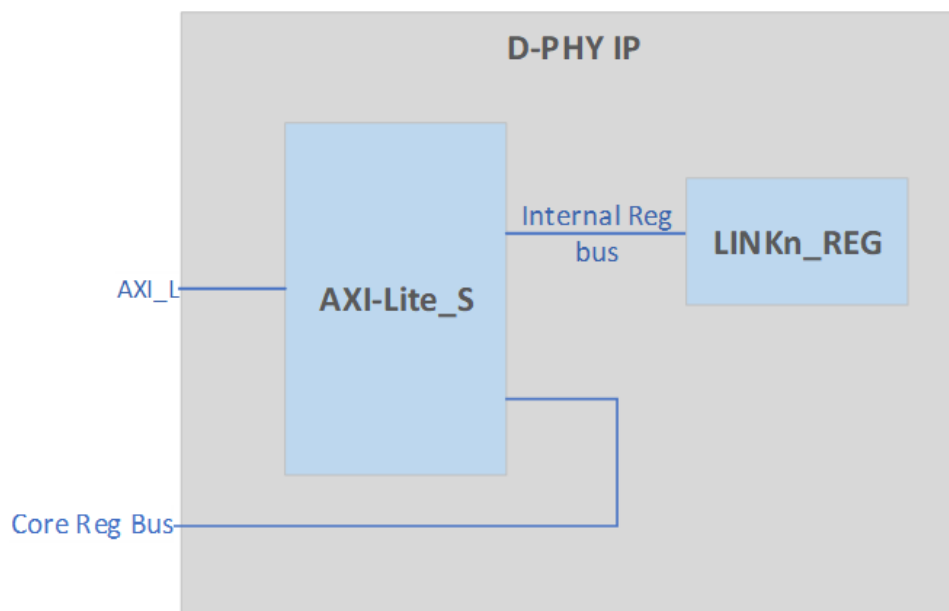
Each link has its own register space, with additional space reserved for connecting to an external agent. Those registers in the mirrored addresses are shared by all links. For an example of these mirrored registers, refer to the topic. For the D-PHY IP design example, the reserved space is used for TG registers as shown below:

Table 27. D-PHY IP Register Map for Design Example

Start	End	Link Number	Register Space
0x000	0x07F	0	D-PHY IP registers for Link 0
0x080	0x0FF		D-PHY IP shared (mirrored)
0x100	0x17F		TG top level registers mirrored across all links (mirrored)
0x180	0x1FF		TG registers for Link 0
0x200	0x27F	1	D-PHY IP registers for Link 1
0x280	0x2FF		D-PHY IP shared (mirrored)
0x300	0x37F		TG top level registers mirrored across all links (mirrored)
0x380	0x3FF		TG registers for Link 1
0x400	0x47F	2	D-PHY IP registers for Link 2
0x480	0x4FF		D-PHY IP shared (mirrored)
0x500	0x57F		TG top level registers mirrored across all links (mirrored)
0x580	0x5FF		TG registers for Link 2
0x600	0x67F	3	D-PHY IP registers for Link 3
0x680	0x6FF		D-PHY IP shared (mirrored)
0x700	0x77F		TG top level registers mirrored across all links (mirrored)
0x780	0x7FF		TG registers for Link 3
0x800	0x87F	4	D-PHY IP registers for Link 4
0x880	0x8FF		D-PHY IP shared (mirrored)
0x900	0x97F		TG top level registers mirrored across all links (mirrored)
0x980	0x9FF		TG registers for Link 4
0xA00	0xA7F	5	D-PHY IP registers for Link 5
0xA80	0xAFF		D-PHY IP shared (mirrored)
0xB00	0xB7F		TG top level registers mirrored across all links (mirrored)
0xB80	0xBFF		TG registers for Link 5
0xC00	0xC7F	6	D-PHY IP registers for Link 6
0xC80	0xCFF		D-PHY IP shared (mirrored)
0xD00	0xD7F		TG top level registers mirrored across all links (mirrored)
0xD80	0xDFF		TG registers for Link 6

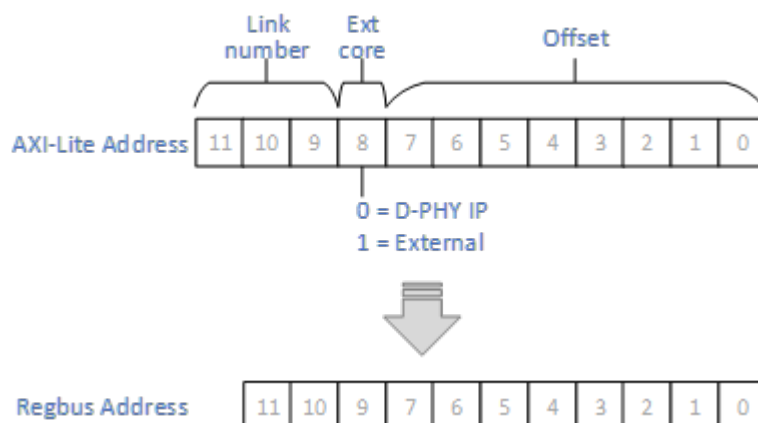
The external register space is accessed using a simple register bus as shown below:

Figure 26. Core Register Bus Diagram



The AXI-Lite client on the D-PHY IP does sub-decode by looking at bit[8] of the AXI-Lite address. The register bus address bits are mapped as shown below:

Figure 27. AXI-Lite Bus Address to Register Bus Address



The waveform diagram below shows AXI-Lite write and read to external registers:

Figure 28. AXI-Lite Write to External Register Waveform

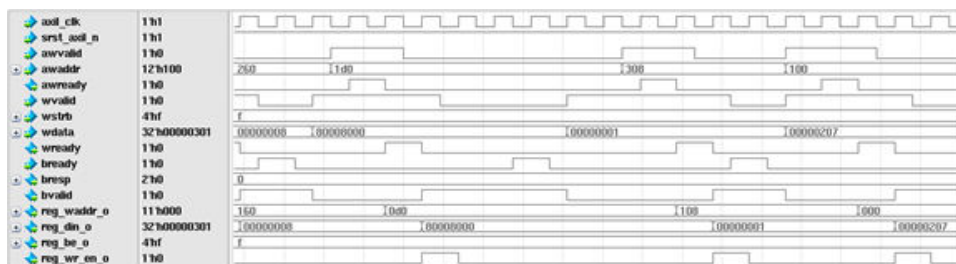
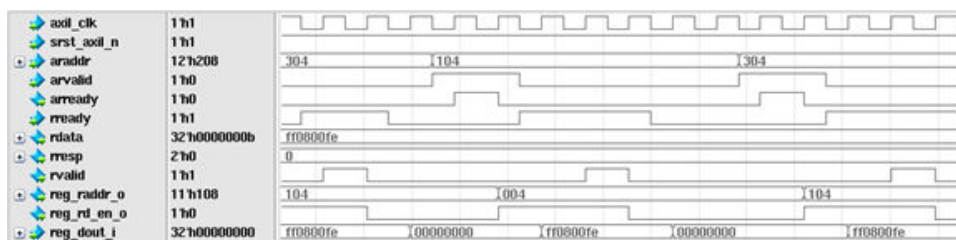


Figure 29. AXI-Lite Read from External Register Waveform



8.2. Register Maps

The following sections list the registers for the IP.

8.2.1. D-PHY IP Registers

The table below provides a register list of a D-PHY link in the IP.

The presence of some registers depends on the link configuration. TX registers exist only when the D-PHY link is configured as TX; RX registers exist only when the link is configured as RX. Any writes to addresses that do not exist are ignored. Reads return 0s.

Table 28. D-PHY IP Register List

Register	Offset	Width	Access	Reset	Description
IP_ID	0x00	8	Read Only	0x00	IP Version ID
IP_CAP	0x01	8	Read Only	Param	Capability Register 0
D0_CAP	0x03	8	Read Only	0x06	Lane 0 Capability
DN_CAP	0x04	8	Read Only	0x02	Lane 1-N Capability
RX_CAP	0x08	8	Read Only	Param	Rx Capability Register
TX_CAP	0x0C	8	Read Only	Param	Tx Capability Register
TX_PREAMBLE_LEN	0x0D	8	Read Write	Param	Tx Preamble Control
D-PHY_CSR	0x10	8	Read Write	0x01	Soft reset / Enable

continued...

Register	Offset	Width	Access	Reset	Description
TX_CLK_LANE_PS	0x11	8	Read Only	Param	Tx Clock Phase Shift
RX_DLANE_ERR	0x12	8	Read Only	0x00	Data lane 0-7 error status
SKEW_CAL_LEN_B0	0x14	8	Read Only	Param	Skew calibration length [7:0] - used by TX for inti skew generation when SKEW_CAL_EN=1
SKEW_CAL_LEN_B1	0x15	8	Read Only	Param	Skew calibration length [15:8] - used by TX for init skew generation when SKEW_CAL_EN=1
SKEW_CAL_LEN_B2	0x16	8	Read Only	Param	Skew calibration length [23:16] - used by TX for init skew generation when SKEW_CAL_EN=1
SKEW_CAL_LEN_B3	0x17	8	Read Only	Param	Skew calibration length [31:24] - used by TX for init skew generation when SKEW_CAL_EN=1
ALT_CAL_LEN_B0	0x18	8	Read Only	Param	Alternate calibration length [7:0] - used by TX for alternate cal generation when ALT_CAL_EN=1
ALT_CAL_LEN_B1	0x19	8	Read Only	Param	Alternate calibration length [15:8] - used by TX for alternate cal generation when ALT_CAL_EN=1
ALT_CAL_LEN_B2	0x1A	8	Read Only	Param	Alternate calibration length [23:16] - used by TX for alternate cal generation when ALT_CAL_EN=1
ALT_CAL_LEN_B3	0x1B	8	Read Only	Param	Alternate calibration length [31:24] - used by TX for alternate cal generation when ALT_CAL_EN=1
CLK_CSR	0x1C	8	Read Write	0x01	Clock lane CSR.
CLK_STATUS	0x1D	8	Read Only	0x00	Clock Status
DLANE_CSR_0	0x20	8	Read Write	Param	Data Lane 0 CSR 0
DLANE_STATUS_0	0x21	8	Read Only	0x00	
RX_DLANE_DESKEW_DELAY_0	0x22	8	Read Write *	Param	RX Data lane deskew delay 0
RX_DLANE_ERR_0	0x23	8	Read Write	0x00	Data Lane 0 error status register (RX)
DLANE_CSR_1	0x24	8	Read Write	Param	Data Lane 1 CSR 0
DLANE_STATUS_1	0x25	8	Read Only	0x00	
RX_DLANE_DESKEW_DELAY_1	0x26	8	Read Write *	Param	RX Data lane deskew delay 1
RX_DLANE_ERR_1	0x27	8	Read Write	0x00	Data Lane 1 error status register (RX)
DLANE_CSR_2	0x28	8	Read Write	Param	Data Lane 2 CSR 0
DLANE_STATUS_2	0x29	8	Read Only	0x00	
RX_DLANE_DESKEW_DELAY_2	0x2A	8	Read Write *	Param	RX Data lane deskew delay 2
RX_DLANE_ERR_2	0x2B	8	Read Write	0x00	Data Lane 2 error status register (RX)
DLANE_CSR_3	0x2C	8	Read Write	Param	Data Lane 3 CSR 0
DLANE_STATUS_3	0x2D	8	Read Only	0x00	
continued...					

Register	Offset	Width	Access	Reset	Description
RX_DLANE_DESKEW_DELAY_3	0x2E	8	Read Write *	Param	RX Data lane deskew delay 3
RX_DLANE_ERR_3	0x2F	8	Read Write	0x00	Data Lane 3 error status register (RX)
DLANE_CSR_4	0x30	8	Read Write	Param	Data Lane 4 CSR 0
DLANE_STATUS_4	0x31	8	Read Only	0x00	
RX_DLANE_DESKEW_DELAY_4	0x32	8	Read Write *	Param	RX Data lane deskew delay 4
RX_DLANE_ERR_4	0x33	8	Read Write	0x00	Data Lane 4 error status register (RX)
DLANE_CSR_5	0x34	8	Read Write	Param	Data Lane 5 CSR 0
DLANE_STATUS_5	0x35	8	Read Only	0x00	
RX_DLANE_DESKEW_DELAY_5	0x36	8	Read Write *	Param	RX Data lane deskew delay 5
RX_DLANE_ERR_5	0x37		Read Write	0x00	Data Lane 5 error status register (RX)
DLANE_CSR_6	0x38	8	Read Write	Param	Data Lane 6 CSR 0
DLANE_STATUS_6	0x39	8	Read Only	0x00	
RX_DLANE_DESKEW_DELAY_6	0x3A	8	Read Write *	Param	RX Data lane deskew delay 6
RX_DLANE_ERR_6	0x3B	8	Read Write	0x00	Data Lane 6 error status register (RX)
DLANE_CSR_7	0x3C	8	Read Write	Param	Data Lane 7 CSR 0
DLANE_STATUS_7	0x3D	8	Read Only	0x00	
RX_DLANE_DESKEW_DELAY_7	0x3E	8	Read Write *	Param	RX Data lane deskew delay 7
RX_DLANE_ERR_7	0x3F	8	Read Write	0x00	Data Lane 7 error status register (RX)
TX_LPX	0x40	8	Read Write *	Param	TX_LPX
TX_HS_EXIT	0x41	8	Read Write *	Param	TX_HS_EXIT
TX_LP_EXIT	0x42	8	Read Write *	Param	TX_LP_EXIT
TX_CLK_PREPARE	0x44	8	Read Write *	Param	TX_CLK_PREPARE
TX_CLK_TRAIL	0x45	8	Read Write *	Param	TX_CLK_TRAIL
TX_CLK_ZERO	0x46	8	Read Write *	Param	TX_CLK_ZERO
TX_CLK_POST	0x47	8	Read Write *	Param	TX_CLK_POST
TX_CLK_PRE	0x48	8	Read Write *	Param	TX_CLK_PRE
TX_HS_PREPARE	0x49	8	Read Write *	Param	TX_HS_PREPARE
TX_HS_ZERO	0x4A	8	Read Write *	Param	TX_HS_ZERO
TX_HS_TRAIL	0x4C	8	Read Write *	Param	TX_HS_TRAIL
TX_INIT	0x4E	8	Read Write *	Param	TX_INIT
TX_WAKE	0x4F	8	Read Write *	Param	TX_WAKE
RX_CLK_LOSS_DETECT	0x50	8	Read Write *	Param	RX_CLK_LOSS_DETECT
RX_CLK_SETTLE	0x51	8	Read Write *	Param	RX_CLK_SETTLE
continued...					

Register	Offset	Width	Access	Reset	Description
RX_HS_SETTLE	0x52	8	Read Write *	Param	RX_HS_SETTLE
RX_INIT	0x54	8	Read Write *	Param	RX_INIT
RX_CLK_POST	0x55	8	Read Write *	Param	RX_CLK_POST
RX_CAL_REG_CTRL	0x60	8	Read Write	0x00	Rx Capability Register
RX_CAL_STATUS_D-PHY	0x61	8	Read Only	0x00	D-PHY Calibration Status Register
RX_CAL_SKEW_W_START_MUX	0x62	8	Read Only	0x00	Window start delay settings for skew calibration for lane CAL_REG_MUXSEL
RX_CAL_SKEW_W_END_MUX	0x63	8	Read Only	0x00	Window end delay settings for skew calibration for lane CAL_REG_MUXSEL
RX_CAL_ALT_W_START_MUX	0x64	8	Read Only	0x00	Window start delta from alternate calibration for lane CAL_REG_MUXSEL
RX_CAL_ALT_W_END_MUX	0x65	8	Read Only	0x00	Window end delta from alternate calibration for lane CAL_REG_MUXSEL
RX_DESKEW_DELAY_MUX	0x66	8	Read Only	0x00	RX deskew delay for lane CAL_REG_MUXSEL
RX_CAL_STATUS_LANE_MUX	0x67	8	Read Only	0x00	Calibration status for lane CAL_REG_MUXSEL
PRBS_INIT_0	0x68	8	Read Write *	Param	PRBS9 seed value for data lane 0
PRBS_INIT_1	0x69	8	Read Write *	Param	PRBS9 seed value for data lane 1
PRBS_INIT_2	0x6A	8	Read Write *	Param	PRBS9 seed value for data lane 2
PRBS_INIT_3	0x6B	8	Read Write *	Param	PRBS9 seed value for data lane 3
PRBS_INIT_4	0x6C	8	Read Write *	Param	PRBS9 seed value for data lane 4
PRBS_INIT_5	0x6D	8	Read Write *	Param	PRBS9 seed value for data lane 5
PRBS_INIT_6	0x6E	8	Read Write *	Param	PRBS9 seed value for data lane 6
PRBS_INIT_7	0x6F	8	Read Write *	Param	PRBS9 seed value for data lane 7
TX_TM_CONTROL	0x70	8	Read Write	0x00	TX test mode control register
TX_MNL_IO_0	0x72	8	Read Write	0x00	TX Manual I/O control register 0
TX_MNL_D_LP_EN	0x73	8	Read Write	0x00	TX Manual I/O Data Lane LP (HSb) Control for Data lanes
RX_TM_CONTROL	0x78	8	Read Write	0x00	RX test mode control register

8.2.1.1. IP_ID

Offset: 0x00

Default: 0x00

Description: IP version ID

Bit	Name	Access	Description
7:0	IP_ID	Read Only	IP version ID

8.2.1.2. IP_CAP

Offset: 0x01
Default: IP Param
Description: Capability Register 0

Bit	Name	Access	Description
5:3	IP_CAP_NLANES	Read Only	Number of lanes 000 = 1 001 = 2 010 = 4 011 = 8 1XX = reserved
2:1	IP_CAP_PPI_WIDTH	Read Only	PPI data width 00 = 8 01 = 16 1X = reserved
0	IP_CAP_ROLE	Read Only	D-PHY Lane Interconnect Side 1 = TX 0 = RX

8.2.1.3. D0_CAP

Offset: 0x03
Default: 0x06
Description: Lane 0 Capability

Bit	Name	Access	Description
4:3	D0_CAP_REV_CAP	Read Only	Reverse direction ESC mode feature support 00 - None 01 - Events only 11 - All (including LPDT)
2:1	D0_CAP_FWD_ESC_CAP	Read Only	Forward direction ESC mode feature support 00 - None 01 - Events only 11 - All (including LPDT)
0	D0_CAP_HS_CAP	Read Only	HS capability 0 - Forward only 1 - Forward and reverse (not currently supported)

8.2.1.4. DN_CAP

Offset: 0x04
Default: 0x02
Description: Lane 1-N Capability

Bit	Name	Access	Description
4:3	DN_CAP_REV_CAP	Read Only	Reverse direction ESC mode feature support 00 - None 01 - Events only 11 - All (including LPDT)
2:1	DN_CAP_FWD_ESC_CAP	read Only	Forward direction ESC mode feature support 00 - None 01 - Events only 11 - All (including LPDT)
0	DN_CAP_HS_CAP	Read Only	HS capability 0 - Forward only 1 - Forward and reverse (not currently supported)

8.2.1.5. RX_CAP

Offset: 0x08
 Default: IP Param
 Description: RX Capability Register

Bit	Name	Access	Description
3	RX_CAP_PERIODIC_SKEW_CAL	Read Only	Periodic skew calibration
2	RX_CAP_PREAMBLE	Read Only	Preamble
1	RX_CAP_ALT_CAL	Read Only	Alternate calibration
0	RX_CAP_SKEW_CAL	Read Only	Skew calibration

8.2.1.6. TX_CAP

Offset: 0x0C
 Default: IP Param
 Description: TX Capability Register

Bit	Name	Access	Description
4:3	TX_CAP_EQ_MODE	Read Only	Tx Equalization mode 00 - OFF 01 - MED_LP 10 - HI_LP 11 - MED_CZ
2	TX_CAP_PREAMBLE	Read Only	Preamble
1	TX_CAP_ALT_CAL	Read Only	Alternate calibration
0	TX_CAP_SKEW_CAL	Read Only	Skew calibration

8.2.1.7. TX_PREAMBLE_LEN

Offset: 0x0D
Default: IP Param
Description: TX Preamble Control

Bit	Name	Access	Description
4:1	TX_PREAMBLE_LEN_PRE AMLBE_LEN	Read Write	Preamble length 4'h0 - 32 4'h1 - 64 4'h2 - 96 ... 4'hE - 480 4'hF - 512
0	TX_PREAMBLE_LEN_PRE AMBLE_EN	Read Write	Preamble Enable 0 - Disable 1 - Enable

8.2.1.8. D-PHY_CSR

Offset: 0x10
Default: 0x01
Description: Soft reset / Enable

Bit	Name	Access	Description
1	D-PHY_CSR_PLL_LOCK	Read Only	PLL lock signal
0	D-PHY_CSR_Enable	Read Write	D-PHY Enable

8.2.1.9. TX_CLK_LANE_PS

Offset: 0x11
Default: IP Param
Description: TX Clock Phase Shift

Bit	Name	Access	Description
5:0	TX_CLK_LANE_PS	Read Only	Tx Clock Phase Shift Sets the phase shift of the clock lane relative to the data lanes. 1 UI is equivalent to 64 steps. Default is 32, shifting clock by 1/2 UI.

8.2.1.10. RX_DLANE_ERR

Offset: 0x12
 Default: 0x00
 Description: Data lane 0-7 error status

Bit	Name	Access	Description
7:0	RX_DLANE_ERR	Read Only	Data lane 0-7 error status Derived from RX_DLANE_ERR_0 bit N = RX_DLANE_ERR_N [7:0] : Data lane 7 - 0 error status 1 = error 0 = no error

8.2.1.11. SKEW_CAL_LEN_B0

Offset: 0x14
 Default: IP Param
 Description: Skew calibration length [7:0] - used by TX for inti skew generation when SKEW_CAL_EN=1.

Bit	Name	Access	Description
7:0	SKEW_CAL_LEN_B0	Read Only	Skew calibration length [7:0] - used by TX for inti skew generation when SKEW_CAL_EN=1.

8.2.1.12. SKEW_CAL_LEN_B1

Offset: 0x15
 Default: IP Param
 Description: Skew calibration length [15:8] - used by TX for init skew generation when SKEW_CAL_EN=1.

Bit	Name	Access	Description
7:0	SKEW_CAL_LEN_B1	Read Only	Skew calibration length [15:8] - used by TX for init skew generation when SKEW_CAL_EN=1.

8.2.1.13. SKEW_CAL_LEN_B2

Offset: 0x16
 Default: IP Param
 Description: Skew calibration length [23:16] - used by TX for init skew generation when SKEW_CAL_EN=1.

Bit	Name	Access	Description
7:0	SKEW_CAL_LEN_B2	Read Only	Skew calibration length [23:16] - used by TX for init skew generation when SKEW_CAL_EN=1.

8.2.1.14. SKEW_CAL_LEN_B3

Offset: 0x17
Default: IP Param
Description: Skew calibration length [31:24] - used by TX for init skew generation when SKEW_CAL_EN=1.

Bit	Name	Access	Description
7:0	SKEW_CAL_LEN_B3	Read Only	Skew calibration length [31:24] - used by TX for init skew generation when SKEW_CAL_EN=1.

8.2.1.15. ALT_CAL_LEN_B0

Offset: 0x18
Default: IP Param
Description: Alternate calibration length [7:0] - used by TX for alternate cal generation when ALT_CAL_EN=1.

Bit	Name	Access	Description
7:0	ALT_CAL_LEN_B0	Read Only	Alternate calibration length [7:0] - used by TX for alternate cal generation when ALT_CAL_EN=1.

8.2.1.16. ALT_CAL_LEN_B1

Offset: 0x19
Default: IP Param
Description: Alternate calibration length [15:8] - used by TX for alternate cal generation when ALT_CAL_EN=1.

Bit	Name	Access	Description
7:0	ALT_CAL_LEN_B1	Read Only	Alternate calibration length [15:8] - used by TX for alternate cal generation when ALT_CAL_EN=1.

8.2.1.17. ALT_CAL_LEN_B2

Offset: 0x1A
Default: IP Param
Description: Alternate calibration length [23:16] - used by TX for alternate cal generation when ALT_CAL_EN=1.

Bit	Name	Access	Description
7:0	ALT_CAL_LEN_B2	Read Only	Alternate calibration length [23:16] - used by TX for alternate cal generation when ALT_CAL_EN=1.

8.2.1.18. ALT_CAL_LEN_B3

Offset: 0x1B

Default: IP Param

Description: Alternate calibration length [31:24] - used by TX for alternate cal generation when ALT_CAL_EN=1.

Bit	Name	Access	Description
7:0	ALT_CAL_LEN_B3	Read Only	Alternate calibration length [31:24] - used by TX for alternate cal generation when ALT_CAL_EN=1.

8.2.1.19. CLK_CSR

Offset: 0x1C

Default: 0x01

Description: Clock lane CSR

Bit	Name	Access	Description
0	CLK_CSR_CLK_LANE_EN	Read Write	Enable - when enabling, set this register bit first before setting D-PHY_CSR.Enable to 1.

8.2.1.20. CLK_STATUS

Offset: 0x1D

Default: 0x00

Description:

Bit	Name	Access	Description
0	CLK_STATUS_INIT_DONE	Read Only	Clock lane init done.

8.2.1.21. DLANE_CSR_0

Offset: 0x20

Default: IP Param

Description: Data Lane 0 CSR 0

Bit	Name	Access	Description
4	DLANE_CSR_0_RX_MNL_DESKEW_EN	Read Write	Manual deskew delay enable.
3	DLANE_CSR_0_RX_DESKEW_UPDATE	RWSC	A write of '1' to this register will trigger deskew delay update MNL_DESKEW_EN = 1 - triggers write from RX_DLANE_DESKEW_DELAY_0 MNL_DESKEW_EN = 0 - triggers write from calibration state machine.
0	DLANE_CSR_0_EN	Read Write	Enable - when enabling, set this register bit first before setting D-PHY_CSR.Enable to 1.

8.2.1.22. DLANE_STATUS_0

Offset: 0x21

Default: 0x00

Description:

Bit	Name	Access	Description
0	DLANE_STATUS_0_INIT_DONE	Read Only	Data lane init done For TX with SKEW_CAL_EN (and ALT_CAL_EN) set to 1, this only gets asserted after the calibration is done.

8.2.1.23. RX_DLANE_DESKEW_DELAY_0

Offset: 0x22

Default: IP Param

Description: RX Data lane deskew delay 0

Bit	Name	Access	Description
6:0	RX_DLANE_DESKEW_DELAY_0	Read Write *	RX Data lane deskew delay 0 Manual data Lane 0 deskew delay setting.
Note: * Can be configured to be Read Only during IP generation to save resources.			

8.2.1.24. RX_DLANE_ERR_0

Offset: 0x23

Default: 0x00

Description: Data Lane 0 error status register (RX).

Bit	Name	Access	Description
6	RX_DLANE_ERR_0_CAL_ERR	RW1C	Calibration error.
5	RX_DLANE_ERR_0_CTRL_ERR	RW1C	False control error.
4	RX_DLANE_ERR_0_LPDT_ERR	RW1C	LP transmission sync error.
3	RX_DLANE_ERR_0_ESC_ENTRY_ERR	RW1C	ESC mode entry error.
2	RX_DLANE_ERR_0_EOT_SYNC_ERR	RW1C	EoT sync error.
1	RX_DLANE_ERR_0_SOT_SYNC_ERR	RW1C	SoT sync error.
0	RX_DLANE_ERR_0_SOT_ERR	RW1C	SoT error.

8.2.1.25. DLANE_CSR_1

Offset: 0x24
 Default: IP Param
 Description: Data lane 1 CSR 0

Bit	Name	Access	Description
4	DLANE_CSR_1_RX_MNL_DESKEW_EN	Read Write	Manual deskew delay enable.
3	DLANE_CSR_1_RX_DESKEW_UPDATE	RWSC	A write of '1' to this register will trigger deskew delay update MNL_DESKEW_EN = 1 - triggers write from RX_DLANE_DESKEW_DELAY_1 MNL_DESKEW_EN = 0 - triggers write from calibration state machine.
0	DLANE_CSR_1_EN	Read Write	Enable - when enabling, set this register bit first before setting D-PHY_CSR.Enable to 1.

8.2.1.26. DLANE_STATUS_1

Offset: 0x25
 Default: 0x00
 Description:

Bit	Name	Access	Description
0	DLANE_STATUS_1_INIT_DONE	Read Only	Data lane init done For TX with SKEW_CAL_EN (and ALT_CAL_EN) set to 1, this only gets asserted after the calibration is done.

8.2.1.27. RX_DLANE_DESKEW_DELAY_1

Offset: 0x26
Default: IP Param
Description: RX Data lane deskew delay 1

Bit	Name	Access	Description
6:0	RX_DLANE_DESKEW_DELAY_1	Read Write *	RX Data lane deskew delay 1 Manual data Lane 1 deskew delay setting.
Note: * Can be configured as Read Only during IP generation to save resources.			

8.2.1.28. RX_DLANE_ERR_1

Offset: 0x27
Default: 0x00
Description: Data Lane 1 error status register (RX)

Bit	Name	Access	Description
6	RX_DLANE_ERR_1_CAL_ERR	RW1C	Calibration error.
5	RX_DLANE_ERR_1_CTRL_ERR	RW1C	False control error.
4	RX_DLANE_ERR_1_LPDT_ERR	RW1C	LP transmission sync error.
3	RX_DLANE_ERR_1_ESC_ENTRY_ERR	RW1C	ESC mode entry error.
2	RX_DLANE_ERR_1_EOT_SYNC_ERR	RW1C	EoT sync error.
1	RX_DLANE_ERR_1_SOT_SYNC_ERR	RW1C	SoT sync error.
0	RX_DLANE_ERR_1_SOT_ERR	RW1C	SoT error.

8.2.1.29. DLANE_CSR_2

Offset: 0x28
Default: IP Param
Description: Data Lane 2 CSR 0

Bit	Name	Access	Description
4	DLANE_CSR_2_RX_MNL_DESKEW_EN	Read Write	Manual deskew delay enable.
3	DLANE_CSR_2_RX_DESKEW_UPDATE	RWSC	A write of '1' to this register will trigger deskew delay update MNL_DESKEW_EN = 1 - triggers write from RX_DLANE_DESKEW_DELAY_2 MNL_DESKEW_EN = 0 - triggers write from calibration state machine.
0	DLANE_CSR_2_EN	Read Write	Enable - when enabling, set this register bit first before setting D-PHY_CSR.Enable to 1.

8.2.1.30. DLANE_STATUS_2

Offset: 0x29

Default: 0x00

Description:

Bit	Name	Access	Description
0	DLANE_STATUS_2_INIT_DONE	Read Only	Data lane init done. For TX with SKEW_CAL_EN (and ALT_CAL_EN) set to 1, this only gets asserted after the calibration is done.

8.2.1.31. RX_DLANE_DESKEW_DELAY_2

Offset: 0x2A

Default: IP Param

Description: RX Data lane deskew delay 2

Bit	Name	Access	Description
6:0	RX_DLANE_DESKEW_DELAY_2	Read Write *	RX Data lane deskew delay 2. Manual data Lane 2 deskew delay setting.
Note: * Can be configured as Read Only during IP generation to save resources.			

8.2.1.32. RX_DLANE_ERR_2

Offset: 0x2B

Default: 0x00

Description: Data Lane 2 error status register (RX)

Bit	Name	Access	Description
6	RX_DLANE_ERR_2_CAL_ERR	RW1C	Calibration error.
5	RX_DLANE_ERR_2_CTRL_ERR	RW1C	False control error.
4	RX_DLANE_ERR_2_LPDT_ERR	RW1C	LP transmission sync error.
3	RX_DLANE_ERR_2_ESC_ENTRY_ERR	RW1C	ESC mode entry error.
2	RX_DLANE_ERR_2_EOT_SYNC_ERR	RW1C	EoT sync error.
1	RX_DLANE_ERR_2_SOT_SYNC_ERR	RW1C	SoT sync error.
0	RX_DLANE_ERR_2_SOT_ERR	RW1C	SoT error.

8.2.1.33. DLANE_CSR_3

Offset: 0x2C
 Default: IP Param
 Description: Data Lane 3 CSR 0

Bit	Name	Access	Description
4	DLANE_CSR_3_RX_MNL_DESKEW_EN	Read Write	Manual deskew delay enable.
3	DLANE_CSR_3_RX_DESKEW_UPDATE	RWSC	A write of '1' to this register will trigger deskew delay update MNL_DESKEW_EN = 1 - triggers write from RX_DLANE_DESKEW_DELAY_3 MNL_DESKEW_EN = 0 - triggers write from calibration state machine.
0	DLANE_CSR_3_EN	Read Write	Enable - when enabling, set this register bit first before setting D-PHY_CSR.Enable to 1.

8.2.1.34. DLANE_STATUS_3

Offset: 0x2D
 Default: 0x00
 Description:

Bit	Name	Access	Description
0	DLANE_STATUS_3_INIT_DONE	Read Only	Data lane init done. For TX with SKEW_CAL_EN (and ALT_CAL_EN) set to 1, this only gets asserted after the calibration is done.

8.2.1.35. RX_DLANE_DESKEW_DELAY_3

Offset: 0x2E
 Default: IP Param
 Description: RX Data lane deskew delay 3

Bit	Name	Access	Description
6:0	RX_DLANE_DESKEW_DELAY_3	Read Write *	RX Data lane deskew delay 3. Manual data Lane 3 deskew delay setting.
Note: * Can be configured as Read Only during IP generation to save resources.			

8.2.1.36. RX_DLANE_ERR_3

Offset: 0x2F
 Default: 0x00
 Description: Data Lane 3 error status register (RX)

Bit	Name	Access	Description
6	RX_DLANE_ERR_3_CAL_ERR	RW1C	Calibration error.
5	RX_DLANE_ERR_3_CTRL_ERR	RW1C	False control error.
4	RX_DLANE_ERR_3_LPD_T_ERR	RW1C	LP transmission sync error.
3	RX_DLANE_ERR_3_ESC_ENTRY_ERR	RW1C	ESC mode entry error.
2	RX_DLANE_ERR_3_EOT_SYNC_ERR	RW1C	EoT sync error.
1	RX_DLANE_ERR_3_SOT_SYNC_ERR	RW1C	SoT sync error.
0	RX_DLANE_ERR_3_SOT_ERR	RW1C	SoT error

8.2.1.37. DLANE_CSR_4

Offset: 0x30
 Default: IP Param
 Description: Data Lane 4 CSR 0

Bit	Name	Access	Description
4	DLANE_CSR_4_RX_MNL_DESKEW_EN	Read Write	Manual deskew delay enable.
3	DLANE_CSR_4_RX_DESKEW_UPDATE	RWSC	A write of '1' to this register will trigger deskew delay update. MNL_DESKEW_EN = 1 - triggers write from RX_DLANE_DESKEW_DELAY_4 MNL_DESKEW_EN = 0 - triggers write from calibration state machine.
0	DLANE_CSR_4_EN	read Write	Enable - when enabling, set this register bit first before setting D-PHY_CSR.Enable to 1.

8.2.1.38. DLANE_STATUS_4

Offset: 0x31

Default: 0x00

Description:

Bit	Name	Access	Description
0	DLANE_STATUS_4_INIT_DONE	Read Only	Data lane init done For TX with SKEW_CAL_EN (and ALT_CAL_EN) set to 1, this only gets asserted after the calibration is done.

8.2.1.39. RX_DLANE_DESKEW_DELAY_4

Offset: 0x32

Default: IP Param

Description: RX Data lane deskew delay 4

Bit	Name	Access	Description
6:0	RX_DLANE_DESKEW_DELAY_4	Read Write *	RX Data lane deskew delay 4. Manual data Lane 4 deskew delay setting.
Note: * Can be configured as Read Only during IP generation to save resources.			

8.2.1.40. RX_DLANE_ERR_4

Offset: 0x33

Default: 0x00

Description: Data Lane 4 error status register (RX)

Bit	Name	Access	Description
6	RX_DLANE_ERR_4_CAL_ERR	RW1C	Calibration error.
5	RX_DLANE_ERR_4_CTRL_ERR	RW1C	False control error.
4	RX_DLANE_ERR_4_LPDT_ERR	RW1C	LP transmission sync error.
3	RX_DLANE_ERR_4_ESC_ENTRY_ERR	RW1C	ESC mode entry error.
2	RX_DLANE_ERR_4_EOT_SYNC_ERR	RW1C	EoT sync error.
1	RX_DLANE_ERR_4_SOT_SYNC_ERR	RW1C	SoT sync error.
0	RX_DLANE_ERR_4_SOT_ERR	RW1C	SoT error

8.2.1.41. DLANE_CSR_5

Offset: 0x34
 Default: IP Param
 Description: Data Lane 5 CSR 0

Bit	Name	Access	Description
4	DLANE_CSR_5_RX_MNL_DESKEW_EN	Read Write	Manual deskew delay enable.
3	DLANE_CSR_5_RX_DESKEW_UPDATE	RWSC	A write of '1' to this register will trigger deskew delay update. MNL_DESKEW_EN = 1 - triggers write from RX_DLANE_DESKEW_DELAY_5 MNL_DESKEW_EN = 0 - triggers write from calibration state machine.
0	DLANE_CSR_5_EN	Read Write	Enable - when enabling, set this register bit first before setting D-PHY_CSR.Enable to 1.

8.2.1.42. DLANE_STATUS_5

Offset: 0x35
 Default: 0x00
 Description:

Bit	Name	Access	Description
0	DLANE_STATUS_5_INIT_DONE	Read Only	Data lane init done. For TX with SKEW_CAL_EN (and ALT_CAL_EN) set to 1, this only gets asserted after the calibration is done.

8.2.1.43. RX_DLANE_DESKEW_DELAY_5

Offset: 0x36
Default: IP Param
Description: RX Data lane deskew delay 5

Bit	Name	Access	Description
6:0	RX_DLANE_DESKEW_DELAY_5	Read Write *	RX Data lane deskew delay 5. Manual data Lane 5 deskew delay setting.
Note: * Can be configured as Read only during IP generation to save resources.			

8.2.1.44. RX_DLANE_ERR_5

Offset: 0x37
Default: 0x00
Description: Data Lane 5 error status register (RX)

Bit	Name	Access	Description
6	RX_DLANE_ERR_5_CAL_ERR	RW1C	Calibration error.
5	RX_DLANE_ERR_5_CTRL_ERR	RW1C	False control error.
4	RX_DLANE_ERR_5_LPD_T_ERR	RW1C	LP transmission sync error.
3	RX_DLANE_ERR_5_ESC_ENTRY_ERR	RW1C	ESC mode entry error.
2	RX_DLANE_ERR_5_EOT_SYNC_ERR	RW1C	EoT sync error.
1	RX_DLANE_ERR_5_SOT_SYNC_ERR	RW1C	SoT sync error.
0	RX_DLANE_ERR_5_SOT_ERR	RW1C	SoT error.

8.2.1.45. DLANE_CSR_6

Offset: 0x38
Default: IP Param
Description: Data Lane 6 CSR 0

Bit	Name	Access	Description
4	DLANE_CSR_6_RX_MNL_DESKEW_EN	Read Write	Manual deskew delay enable.
3	DLANE_CSR_6_RX_DESKEW_UPDATE	RWSC	A write of '1' to this register will trigger deskew delay update. MNL_DESKEW_EN = 1 - triggers write from RX_DLANE_DESKEW_DELAY_6 MNL_DESKEW_EN = 0 - triggers write from calibration state machine.
0	DLANE_CSR_6_EN	Read Write	Enable - when enabling, set this register bit first before setting D-PHY_CSR.Enable to 1.

8.2.1.46. DLANE_STATUS_6

Offset: 0x39

Default: 0x00

Description:

Bit	Name	Access	Description
0	DLANE_STATUS_6_INIT_DONE	Read Only	Data lane init done. For TX with SKEW_CAL_EN (and ALT_CAL_EN) set to 1, this only gets asserted after the calibration is done.

8.2.1.47. RX_DLANE_DESKEW_DELAY_6

Offset: 0x3A

Default: IP Param

Description: RX Data lane deskew delay 6

Bit	Name	Access	Description
6:0	RX_DLANE_DESKEW_DELAY_6	Read Write *	RX Data lane deskew delay 6. Manual data Lane 6 deskew delay setting.
Note: * Can be configured as Read Only during IP generation to save resources.			

8.2.1.48. RX_DLANE_ERR_6

Offset: 0x3B

Default: 0x00

Description: Data Lane 6 error status register (RX)

Bit	Name	Access	Description
6	RX_DLANE_ERR_6_CAL_ERR	RW1C	Calibration error.
5	RX_DLANE_ERR_6_CTRL_ERR	RW1C	False control error.
4	RX_DLANE_ERR_6_LPDT_ERR	RW1C	LP transmission sync error.
3	RX_DLANE_ERR_6_ESC_ENTRY_ERR	RW1C	ESC mode entry error.
2	RX_DLANE_ERR_6_EOT_SYNC_ERR	RW1C	EoT sync error.
1	RX_DLANE_ERR_6_SOT_SYNC_ERR	RW1C	SoT sync error.
0	RX_DLANE_ERR_6_SOT_ERR	RW1C	SoT error.

8.2.1.49. DLANE_CSR_7

Offset: 0x3C
 Default: IP Param
 Description: Data Lane 7 CSR 0

Bit	Name	Access	Description
4	DLANE_CSR_7_RX_MNL_DESKEW_EN	Read Write	Manual deskew delay enable.
3	DLANE_CSR_7_RX_DESKEW_UPDATE	RWSC	A write of '1' to this register will trigger deskew delay update MNL_DESKEW_EN = 1 - triggers write from RX_DLANE_DESKEW_DELAY_7 MNL_DESKEW_EN = 0 - triggers write from calibration state machine.
0	DLANE_CSR_7_EN	Read Write	Enable - when enabling, set this register bit first before setting D-PHY_CSR.Enable to 1.

8.2.1.50. DLANE_STATUS_7

Offset: 0x3D
 Default: 0x00
 Description:

Bit	Name	Access	Description
0	DLANE_STATUS_7_INIT_DONE	Read Only	Data lane init done. For TX with SKEW_CAL_EN (and ALT_CAL_EN) set to 1, this only gets asserted after the calibration is done.

8.2.1.51. RX_DLANE_DESKEW_DELAY_7

Offset: 0x3E
 Default: Ip Param
 Description: RX Data lane deskew delay 7

Bit	Name	Access	Description
6:0	RX_DLANE_DESKEW_DELAY_7	Read Write *	RX Data lane deskew delay 7. Manual data Lane 7 deskew delay setting.
Note: * Can be configured as Read Only during IP generation to save resources.			

8.2.1.52. RX_DLANE_ERR_7

Offset: 0x3F
 Default: 0x00
 Description: Data Lane 7 error status register (RX)

Bit	Name	Access	Description
6	RX_DLANE_ERR_7_CAL_ERR	RW1C	Calibration error.
5	RX_DLANE_ERR_7_CTRL_ERR	RW1C	False control error.
4	RX_DLANE_ERR_7_LPDT_ERR	RW1C	LP transmission sync error.
3	RX_DLANE_ERR_7_ESC_ENTRY_ERR	RW1C	ESC mode entry error.
2	RX_DLANE_ERR_7_EOT_SYNC_ERR	RW1C	EoT sync error.
1	RX_DLANE_ERR_7_SOT_SYNC_ERR	RW1C	SoT sync error.
0	RX_DLANE_ERR_7_SOT_ERR	RW1C	SoT error.

8.2.1.53. TX_LPX

Offset: 0x40
 Default: IP Param
 Description: TX_LPX

Bit	Name	Access	Description
6:0	TX_LPX	Read Write *	TX_LPX.
continued...			

Bit	Name	Access	Description
			Transmitted length of any Low-Power state period. T_{LPX} is an internal PHY timing parameter. $T_{CLK-PREPARE}$ is an external parameter, which can differ from TLPX.
Note: * Can be configured as Read Only during IP generation to save resources.			

8.2.1.54. TX_HS_EXIT

Offset: 0x41
Default: IP Param
Description: TX_HS_EXIT

Bit	Name	Access	Description
7:0	TX_HS_EXIT	Read Write *	TX_HS_EXIT. Time that the transmitter drives LP-11 following a HS burst.
Note: * Can be configured as Read Only during IP generation to save resources.			

8.2.1.55. TX_LP_EXIT

Offset: 0x42
Default: IP Param
Description: TX_LP_EXIT

Bit	Name	Access	Description
7:0	TX_LP_EXIT	Read Write *	TX_LP_EXIT. Time that the transmitter drives LP-11 between any LP sequences, or between an LP sequence and a HS burst.
Note: * Can be configured as Read Only during IP generation to save resources.			

8.2.1.56. TX_CLK_PREPARE

Offset: 0x44
Default: IP Param
Description: TX_CLK_PREPARE

Bit	Name	Access	Description
5:0	TX_CLK_PREPARE	Read Write *	TX_CLK_PREPARE Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.
continued...			

Bit	Name	Access	Description
			Delay computation (approx): $T_{CLK-PREPARE} = (TX_CLK_PREPARE + 2) * Core_CLK_period.$
Note: * Can be configured as Read Only during IP generation to save resources.			

8.2.1.57. TX_CLK_ZERO

Offset: 0x46
 Default: IP Param
 Description: TX_CLK_ZERO

Bit	Name	Access	Description
6:0	TX_CLK_ZERO	Read Write *	TX_CLK_ZERO. Time that the transmitter drives the HS-0 state prior to starting the Clock. Delay computation (approx): (+ TXFIFO_LAT is intended) $T_{CLK-ZERO} = (TX_CLK_ZERO + 2 + TXFIFO_LAT) * Core_CLK_period$
Note: * Can be configured as Read Only during IP generation to save resources.			

8.2.1.58. TX_CLK_POST

Offset: 0x47
 Default: IP Param
 Description: TX_CLK_POST

Bit	Name	Access	Description
7:0	TX_CLK_POST	Read Write *	TX_CLK_POST. Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP mode. Interval is defined as the period from the end of THS-TRAIL to the beginning of TCLK-TRAIL. Delay computation (approx) : (+ TXFIFO_LAT is intended) $T_{CLK-POST} = (TX_CLK_POST + 2 + TXFIFO_LAT) * Core_CLK_period$
Note: * Can be configured as Read Only during IP generation to save resources.			

8.2.1.59. TX_CLK_PRE

Offset: 0x48
 Default: IP Param
 Description: TX_CLK_PRE

Bit	Name	Access	Description
3:0	TX_CLK_PRE	Read Write *	TX_CLK_PRE. Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode. Delay computation: $T_{CLK-PRE} = (TX_CLK_PRE + 2 - TXFIFO_LAT) * Core_CLK_period$ Aligned to data lanes' next ESC clock edge.
Note: * Can be configured as Read Only during IP generation to save resources.			

8.2.1.60. TX_HS_PREPARE

Offset: 0x49
Default: IP Param
Description: TX_HS_PREPARE

Bit	Name	Access	Description
5:0	TX_HS_PREPARE	Read Write *	TX_HS_PREPARE Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission. Delay computation (approx): $T_{HS-PREPARE} = (TX_HS_PREPARE + 2) * Core_CLK_period$
Note: * Can be configured as Read Only during IP generation to save resources.			

8.2.1.61. TX_HS_ZERO

Offset: 0x4A
Default: IP Param
Description: TX_HS_ZERO

Bit	Name	Access	Description
7:0	TX_HS_ZERO	Read Write *	TX_HS_ZERO. Time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence. Delay computation (approx): (+ TXFIFO_LAT is intended) $T_{HS-ZERO} = (TX_HS_ZERO + 4 + TXFIFO_LAT) * Core_CLK_period + (PPI_16 ? 8UIs : 0)$
Note: * Can be configured as Read Only during IP generation to save resources.			

8.2.1.62. TX_HS_TRAIL

Offset: 0x4C
 Default: IP Param
 Description: TX_HS_TRAIL

Bit	Name	Access	Description
7:0	TX_HS_TRAIL	Read Write *	TX_HS_TRAIL. Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst. Delay computation (approx): $T_{HS-TRAIL} = (TX_HS_TRAIL + 1) * Core_CLK_period - (TXFIFO_LAT) * CORE_CLK_period$.
Note: * Can be configured as Read Only during IP generation to save resources.			

8.2.1.63. TX_INIT

Offset: 0x4E
 Default: IP Param
 Description: TX_INIT

Bit	Name	Access	Description
7:0	TX_INIT	Read Write *	TX_INIT
Note: * Can be configured as Read Only during IP generation to save resources.			

8.2.1.64. TX_WAKE

Offset: 0x4F
 Default: IP Param
 Description: TX_WAKE

Bit	Name	Access	Description
7:0	TX_WAKE	Read Write *	TX_WAKE
Note: * Can be configured as Read Only during IP generation to save resources.			

8.2.1.65. RX_CLK_LOSS_DETECT

Offset: 0x50
 Default: IP Param
 Description: RX PCS Clock Loss Detect

Bit	Name	Access	Description
7:0	RX_CLK_LOSS_DETECT	Read Write *	<p>RX PCS Clock Loss Detect.</p> <p>Timeout for D-PHY PCS to detect absence of Clock transitions and deassert RxClkActiveHS on the PPI bus. This is different from the D-PHY specification TCLK-MISS. Min value should be equal to 3 x RX_CLK-period (in ns).</p> <p>Delay computations (approx):</p> <p>- $T_{RX_CLK_LOSS_DETECT} = (RX_CLK_LOSS_DETECT + 6) * Core_CLK_period$.</p>
Note: * Can be configured as Read Only during IP generation to save resources.			

8.2.1.66. RX_CLK_SETTLE

Offset: 0x51
 Default: IP Param
 Description: RX_CLK_SETTLE

Bit	Name	Access	Description
7:0	RX_CLK_SETTLE	Read Write *	<p>RX_CLK_SETTLE</p> <p>Time interval during which the HS receiver should ignore any Clock Lane HS transitions, starting from the beginning of TCLK-PREPARE.</p> <p>Delay computation (approx):</p> <p>$T_{RX_CLK_SETTLE} = (RX_CLK_SETTLE + 6) * Core_CLK_period + 2 * RX_CLK_period$</p>
Note: * Can be configured as Read Only during IP generation to save resources.			

8.2.1.67. RX_HS_SETTLE

Offset: 0x52
 Default: IP Param
 Description: RX_HS_SETTLE

Bit	Name	Access	Description
7:0	RX_HS_SETTLE	Read Write *	<p>RX_HS_SETTLE</p> <p>Time interval during which the HS receiver shall ignore any Data Lane HS transitions, starting from the beginning of THS-PREPARE. The HS receiver shall ignore any Data Lane transitions before the minimum value, and the HS receiver shall respond to any Data Lane transitions after the minimum val</p> <p>Delay computation (approx):</p> <p>$T_{HS_SETTLE} = (RX_HS_SETTLE + 7) * Core_CLK_period + (4-4) * RX_CLK_period$.</p>
Note: * Can be configured as Read Only during IP generation to save resources.			

8.2.1.68. RX_INIT

Offset: 0x52
 Default: IP Param
 Description: RX_INIT

Bit	Name	Access	Description
7:0	RX_INIT	Read Write *	RX_INIT After power-up, the RX D-PHY shall be initialized when the TX D-PHY drives a Stop State (LP-11) for a period longer than T_{INIT} . RX side shall ignore all Line states prior to this Initialization period.
Note: * Can be configured as Read Only during IP generation to save resources.			

8.2.1.69. RX_CLK_POST

Offset: 0x55
 Default: IP Param
 Description: RX_CLK_POST

Bit	Name	Access	Description
7:0	RX_CLK_POST	Read Write *	RX_CLK_POST This is only used for continuous clock mode. Protocol specifies the minimum number of clock cycles required after end of data transmission before it is safe to gate the Rx Clock for periodic Rcomp. Delay computation (approx): $T_{RX-CLK_POST} = (RX_CLK_POST + 3) * RX_CLK_period + 5 * Core_CLK_period$.
Note: * Can be configured as Read Only during IP generation to save resources.			

8.2.1.70. RX_CAL_REG_CTRL

Offset: 0x60
 Default: IP Param
 Description: RX Capability Register

Bit	Name	Access	Description
3	RX_CAL_REG_CTRL_CAL_RESET	RWSC	Recalibrate (next skew will be treated as init skew cal) - self clearing for all lanes.
2:0	RX_CAL_REG_CTRL_CAL_REG_MUXSEL	Read Write	Cal/debug reg mux select (0 - 7 for 8 data lanes) index.

8.2.1.71. RX_CAL_STATUS_D-PHY

Offset: 0x61
Default: 0x00
Description: D-PHY Calibration Status Register

Bit	Name	Access	Description
4	RX_CAL_STATUS_D-PHY_ALT_CAL_ERR	Read Only	Alt cal error for 1 or more enabled lanes.
3	RX_CAL_STATUS_D-PHY_PER_SKEW_CAL_ERR	Read Only	Periodic skew cal error for 1 or more enabled lanes.
2	RX_CAL_STATUS_D-PHY_INIT_SKEW_CAL_ERR	Read Only	Init Skew cal error for 1 or more enabled lanes.
1	RX_CAL_STATUS_D-PHY_ALT_CAL_DONE	Read Only	Alt cal complete for all enabled data lanes.
0	RX_CAL_STATUS_D-PHY_SKEW_CAL_DONE	Read Only	Skew cal complete for all enabled data lanes.

8.2.1.72. RX_CAL_SKEW_W_START_MUX

Offset: 0x62
Default: 0x00
Description: Window start delay settings for skew calibration for lane CAL_REG_MUXSEL

Bit	Name	Access	Description
7:0	RX_CAL_SKEW_W_START_MUX	Read Only	Window start delay settings for skew calibration for lane CAL_REG_MUXSEL.

8.2.1.73. RX_CAL_SKEW_W_END_MUX

Offset: 0x63
Default: 0x00
Description: Window end delay settings for skew calibration for lane CAL_REG_MUXSEL

Bit	Name	Access	Description
7:0	RX_CAL_SKEW_W_END_MUX	Read Only	Window end delay settings for skew calibration for lane CAL_REG_MUXSEL.

8.2.1.74. RX_CAL_ALT_W_START_MUX

Offset: 0x64

Default: 0x00

Description: Window start delta from alternate calibration for lane CAL_REG_MUXSEL

Bit	Name	Access	Description
7:0	RX_CAL_ALT_W_START_MUX	Read Only	Window start delta from alternate calibration for lane CAL_REG_MUXSEL.

8.2.1.75. RX_CAL_ALT_W_END_MUX

Offset: 0x65

Default: 0x00

Description: Window end delta from alternate calibration for lane CAL_REG_MUXSEL

Bit	Name	Access	Description
7:0	RX_CAL_ALT_W_END_MUX	Read Only	Window end delta from alternate calibration for lane CAL_REG_MUXSEL.

8.2.1.76. RX_DESKEW_DELAY_MUX

Offset: 0x66

Default: 0x00

Description: RX deskew delay for lane CAL_REG_MUXSEL

Bit	Name	Access	Description
6:0	RX_DESKEW_DELAY_MUX	Read Only	RX deskew delay for lane CAL_REG_MUXSEL - this register is updated during calibration or manual deskew writes - default value is 0 and might not reflect the actual deskew for lane until calibration or manual deskew writes.

8.2.1.77. RX_CAL_STATUS_LANE_MUX

Offset: 0x67

Default: 0x00

Description: Calibration status for lane CAL_REG_MUXSEL

Bit	Name	Access	Description
4	RX_CAL_STATUS_LANE_MUX_ALT_CAL_ERR_LANE	Read Only	Alt cal error .
3	RX_CAL_STATUS_LANE_MUX_PER_SKEW_CAL_ERR_LANE	Read Only	Periodic skew cal error.
2	RX_CAL_STATUS_LANE_MUX_INIT_SKEW_CAL_ERR_LANE	Read Only	Init Skew cal error.
1	RX_CAL_STATUS_LANE_MUX_ALT_CAL_DONE_LANE	Read Only	Alt cal complete.
0	RX_CAL_STATUS_LANE_MUX_SKEW_CAL_DONE_LANE	Read Only	Skew cal complete.

8.2.1.78. PRBS_INIT_0

Offset: 0x68
Default: IP Param
Description: PRBS9 seed value for data lane 0

Bit	Name	Access	Description
7:0	PRBS_INIT_0	Read Write *	PRBS9 seed value for data lane 0. Used by Tx / Rx alt cal and test mode for lane 0.
Note: * Can be configured as Read Only during IP generation to save resources.			

8.2.1.79. PRBS_INIT_1

Offset: 0x69
Default: IP Param
Description: PRBS9 seed value for data lane 1

Bit	Name	Access	Description
7:0	PRBS_INIT_1	Read Write *	PRBS9 seed value for data lane 1. Used by Tx / Rx alt cal and test mode for lane 1.
Note: * Can be configured as Read Only during IP generation to save resources.			

8.2.1.80. PRBS_INIT_2

Offset: 0x6A

Default: IP Param

Description: PRBS9 seed value for data lane 2

Bit	Name	Access	Description
7:0	PRBS_INIT_2	Read Write *	PRBS9 seed value for data lane 2. Used by Tx / Rx alt cal and test mode for lane 2.
<i>Note:</i> * Can be configured as Read Only during IP generation to save resources.			

8.2.1.81. PRBS_INIT_3

Offset: 0x6B

Default: IP Param

Description: PRBS9 seed value for data lane 3

Bit	Name	Access	Description
7:0	PRBS_INIT_3	Read Write *	PRBS9 seed value for data lane 3. Used by Tx / Rx alt cal and test mode for lane 3.
<i>Note:</i> * Can be configured as Read Only during IP generation to save resources.			

8.2.1.82. PRBS_INIT_4

Offset: 0x6C

Default: IP Param

Description: PRBS9 seed value for data lane 4

Bit	Name	Access	Description
7:0	PRBS_INIT_4	Read Write *	PRBS9 seed value for data lane 4. Used by Tx / Rx alt cal and test mode for lane 4.
<i>Note:</i> * Can be configured as Read Only during IP generation to save resources.			

8.2.1.83. PRBS_INIT_5

Offset: 0x6D

Default: IP Param

Description: PRBS9 seed value for data lane 5

Bit	Name	Access	Description
7:0	PRBS_INIT_5	Read Write *	PRBS9 seed value for data lane 5. Used by Tx / Rx alt cal and test mode for lane 5.
<i>Note:</i> * Can be configured as Read Only during IP generation to save resources.			

8.2.1.84. PRBS_INIT_6

Offset: 0x6E
Default: IP Param
Description: PRBS9 seed value for data lane 6

Bit	Name	Access	Description
7:0	PRBS_INIT_6	Read Write *	PRBS9 seed value for data lane 6. Used by Tx / Rx alt cal and test mode for lane 6.
Note: * Can be configured as Read Only during IP generation to save resources.			

8.2.1.85. TX_TM_CONTROL

Offset: 0x70
Default: 0x00
Description: TX test mode control register

Bit	Name	Access	Description
2	TX_TM_CONTROL_TX_TST_CNT_RST	RWSC	TX count reset - write 1 to clear all TX counters - (future enhancement).
1	TX_TM_CONTROL_TX_TM_LOOPBACK_MODE	Read Write	TX HS_TEST loopback mode - (future enhancement).
0	TX_TM_CONTROL_TX_TM_EN	Read Write	TX HS_TEST mode enable - (future enhancement).

8.2.1.86. TX_MNL_IO_0

Offset: 0x72
Default: 0x00
Description: TX Manual IO control register 0

Bit	Name	Access	Description
7:6	TX_MNL_IO_0_HS_DAT_CK	Read Write	Data to be driven to IO dp/dp when in manual HS state (clock lane) 00 - HS0 01 - Clock Pattern (0x55) 10 - Clock Pattern (0xaa) 11 - HS1
5:4	TX_MNL_IO_0_HS_DAT_D	Read Write	Data to be driven to IO dp/dp when in manual HS state (data lane) 00 - HS0 01 - Clock Pattern (0x55) 10 - Clock Pattern (0xaa)
continued...			

Bit	Name	Access	Description
			11 - HS1
3:2	TX_MNL_IO_0_LP_DAT	Read Write	Data to be driven to IO dp/dp when in manual LP state 00 - LP00 01 - LP01 10 - LP10 11 - LP11
1	TX_MNL_IO_0_CLK_LP_EN	Read Write	Clock lane LP (HSb) control 0 - HS 1 - LP
0	TX_MNL_IO_0_CTRL_EN	Read Write	TX manual control of IO state enable. Set to 1 to enable manual control of D-PHY TX IO state.

8.2.1.87. TX_MNL_D_LP_EN

Offset: 0x73
 Default: 0x00
 Description: TX Manual IO Data Lane LP (HSb) Control for Data lanes

Bit	Name	Access	Description
7:0	TX_MNL_D_LP_EN	Read Write	TX Manual IO Data Lane LP (HSb) Control for Data lanes bit b = 0 - Data lane b is HS bit b = 1 - Data lane b is LP.

8.2.1.88. RX_TM_CONTROL

Offset: 0x78
 Default: 0x00
 Description: RX test mode control register

Bit	Name	Access	Description
2	RX_TM_CONTROL_RX_TST_CNT_RST	RWSC	RX count reset - write 1 to clear all TX counters - (future enhancement).
1	RX_TM_CONTROL_RX_TM_LOOPBACK_MODE	Read Write	RX HS_TEST loopback mode - (future enhancement).
0	RX_TM_CONTROL_RX_TM_EN	Read Write	RX HS_TEST mode enable - (future enhancement).

8.2.2. D-PHY Traffic Generator (TG) Registers

Table 29. D-PHY IP Traffic Generator (TG) Register List

Register	Offset	Width	Access	Reset	Description
TG_TOP_CTRL_0	0x100	8	Read Write	0x00	TG top control register 0 (mirrored) - affects all links.
TG_TOP_CTRL_1	0x101	8	Read Write	0x00	TG top control register 1 (mirrored) - affects all links.
TG_TOP_DONE	0x104	8	Read Only	0x00	Test done, 1 bit per link (mirrored).
TG_TOP_FAIL	0x105	8	Read Only	0x00	Test fail, 1 bit per link (mirrored).
TG_TOP_TEST_EN	0x106	8	Read Only	0x00	Internal test enable (decoded), 1 bit per test (mirrored).
TG_TOP_TEST_LINK	0x107	8	Read Only	0x00	Internal test link decoded, 1 bit per link (mirrored).
TARGET_TEST_CNT	0x108	8	Read Write	Param	Target test count.
TCHK_CONTROL	0x180	8	Read Write	0x00	
TCHK_LINK_STATUS	0x184	8	Read Only	0x00	
HS_DONE_LANES	0x185	8	Read Only	0x00	HS done per lane (1 bit per lane).
TCHK_LINK_ERR_STATUS	0x188	8	Read Only	0x00	
LANE_ERROR_SOT_LANES	0x189	8	Read Only	0x00	Lane error SOT/SOT SYNC status per lane.
CAL_ERROR_LANES	0x18A	8	Read Only	0x00	Calibration error status per lane.
HS_ERR_LANES	0x18B	8	Read Only	0x00	HS Data transfer error status per lane.
HS_TEST_CNT	0x18C	8	Read Only	0x00	Number of HS test received for lane N where N is controlled by HS_CNT_MUX.
LPDT_TEST_CNT	0x190	8	Read Only	0x00	Number of LPDT test received.
TRIGGER_TEST_CNT	0x194	8	Read Only	0x00	Number of TRIGGER test received.
ULPS_TEST_CNT	0x198	8	Read Only	0x00	Number of ULPS test received.
TG_RX_OVRD_DATA_PAT	0x1A8	8	Read Only	0x00	
TG_RX_BIT_ERROR_CNT	0x1B0	8	Read Only	0x00	Number of bit error found on lane N where N is controlled by HS_CNT_MUX.
TG_RX_HS_TXFER_CNT	0x1B8	8	Read Only	0x00	HS RX total transfer count per lane (from any lane).
TG_LINK_CONTROL	0x1C0	8		0x00	
TG_INIT_CNT	0x1C4	8	Read Write	0x400	Number of ESC clock cycles for TX INIT.
TG_HS_LEN	0x1C8	8	Read Write	0x00	
TG_LP_LEN	0x1CC	8	Read Write	0x00	
TG_SKEW_CAL	0x1D0	8	Read Write	0x20	Initial skew calibration length in UI (rounded down to number of PPI access).
TG_ALT_CAL	0x1D4	8	Read Write	0x40	Alternate skew calibration length in UI (rounded down to number of PPI access)
TG_PER_SKEW_CAL_LEN	0x1D8	8	Read Write	0x04	

continued...

Register	Offset	Width	Access	Reset	Description
TG_TEST_CNT	0x1E0	8	Read Only	0x00	Number of test round completed by TG.
TG_OVRD_DATA_PAT	0x1E8	8	Read Only	0x00	
TG_TX_HS_TXFER_CNT	0x1F8	8	Read Only	0x00	HS TX total transfer count per lane (on any lane).

8.2.2.1. TG_TOP_CTRL_0

Offset: 0x100

Default: 0x00

Description: TG top control register 0 (mirrored) - affects all links

Bit	Name	Access	Description
6:4	TG_TOP_CTRL_0_TEST_EN_RX	Read Write	Test check enable (1 to enable, 0 to mask) : 0 - all checks 1 - DIR error 2 - HS check error 3 - Calibration error 4 - LPDT error 5 - trigger error 6 - ULPS error 7 - SOT/SOT Sync error
3:1	TG_TOP_CTRL_0_TEST_EN_TX	Read Write	Test enable - sets which test to enable: 0 - all tests 1 - alt cal (only used if TG_ALT_CAL.TG_ALT_CAL_UNMASK=1) 2 - HS test 3 - init skew (only used if TG_INIT_SKEW_CAL.TG_INIT_SKEW_CAL_UNMASK=1) 4 - LPDT_TEST 5 - trigger 6 - preamble 7 - per skew
0	TG_TOP_CTRL_0_TEST_CSR_CTRL_EN	Read Write	Test control enable - when set, CSR control overrides pin input.

8.2.2.2. TG_TOP_CTRL_1

Offset: 0x101

Default: 0x00

Description: TG top control register 1 (mirrored) - affects all links

Bit	Name	Access	Description
4:2	TG_TOP_CTRL_1_TEST_LINK_N	Read Write	When TEST_ALL_LINKS = 0, this register sets which link to test.
1	TG_TOP_CTRL_1_TEST_ALL_LINKS	Read Write	Test all links - when set to 1 all enabled D-PHY links are tested.
0	TG_TOP_CTRL_1_TEST_RESTART	Read Write	Write 1 to restart the test; the new test will start when this register is set back to 0.

8.2.2.3. TG_TOP_DONE

Offset: 0x104
 Default: 0x00
 Description: Test done, 1 bit per link (mirrored)

Bit	Name	Access	Description
7:0	TG_TOP_DONE	Read Only	Test done, 1 bit per link (mirrored) bit[N] -> link N's done bit.

8.2.2.4. TG_TOP_FAIL

Offset: 0x105
 Default: 0x00
 Description: Test fail, 1 bit per link (mirrored)

Bit	Name	Access	Description
7:0	TG_TOP_FAIL	Read Only	Test fail, 1 bit per link (mirrored) bit[N] -> link N's fail bit.

8.2.2.5. TG_TOP_TEST_EN

Offset: 0x106
 Default: 0x00
 Description: Internal test enable (decoded), 1 bit per test (mirrored)

Bit	Name	Access	Description
7:0	TG_TOP_TEST_EN	Read Only	Internal test enable (decoded), 1 bit per test (mirrored) bit[N] = 1 means test N is enabled,

8.2.2.6. TG_TOP_TEST_LINK

Offset: 0x107

Default: 0x00

Description: Internal test link decoded, 1 bit per link (mirrored)

Bit	Name	Access	Description
7:0	TG_TOP_TEST_LINK	Read Only	Internal test link decoded, 1 bit per link (mirrored) bit[N] = 1 means link N's test enable is asserted.

8.2.2.7. TARGET_TEST_CNT

Offset: 0x108

Default: IP Parm

Description: Target test count

Bit	Name	Access	Description
31:0	TARGET_TEST_CNT	Read Write	Target test count.

8.2.2.8. TCHK_CONTROL

Offset: 0x180

Default: 0x00

Description:

Bit	Name	Access	Description
5:3	TCHK_CONTROL_HS_CN T_MUX	Read Write	Set mux sel for HS_TEST_CNT register.
2:0	TCHK_CONTROL_TEST_ LANE_NUM	Read Write	Set number of lanes to test. If set higher than IP's lane numbers, it will test all lanes: 100 - 1 D-lane 101 - 2 D-lanes 110 - 4 D-lanes 111 - 8 D-lanes 0XX - num lanes controlled through test_num pins.

8.2.2.9. TCHK_LINK_STATUS

Offset: 0x184

Default: 0x00

Description:

Bit	Name	Access	Description
4	TCHK_LINK_STATUS_HS_DONE	Read Only	HS done.
3	TCHK_LINK_STATUS_ULPS_DONE	Read Only	ULPS done.
2	TCHK_LINK_STATUS_TRIGGER_DONE	Read Only	Trigger done.
1	TCHK_LINK_STATUS_LPDT_DONE	Read Only	LPDT test done.
0	TCHK_LINK_STATUS_DONE	Read Only	Test done.

8.2.2.10. HS_DONE_LANES

Offset: 0x185
 Default: 0x00
 Description: HS done per lane (1 bit per lane)

Bit	Name	Access	Description
7:0	HS_DONE_LANES	Read Only	HS done per lane (1 bit per lane).

8.2.2.11. TCHK_LINK_ERR_STATUS

Offset: 0x188
 Default: 0x00
 Description:

Bit	Name	Access	Description
7	TCHK_LINK_ERR_STATUS_HS_ERR	Read Only	HS data transfer error.
6	TCHK_LINK_ERR_STATUS_CAL_ERR	Read Only	HS calibration error.
5	TCHK_LINK_ERR_STATUS_LPDT_ERR	Read Only	Error in LPDT test.
4	TCHK_LINK_ERR_STATUS_TRIG_ERR	Read Only	Error in Trigger test.
3	TCHK_LINK_ERR_STATUS_LANE_ERR_CTRL	Read Only	Lane error encountered during test (ESC errors or Control error).
2	TCHK_LINK_ERR_STATUS_ULPS_ERR	Read Only	Error in ULPS test.
1	TCHK_LINK_ERR_STATUS_LANE_ERR_SOT	Read Only	Lane error encountered during test (SOT and SOT SYNC error).
0	TCHK_LINK_ERR_STATUS_FAIL	Read Only	Test Failed.

8.2.2.12. LANE_ERROR_SOT_LANES

Offset: 0x189
 Default: 0x00
 Description: Lane error SOT/SOT SYNC status per lane

Bit	Name	Access	Description
7:0	LANE_ERROR_SOT_LANES	Read Only	Lane error SOT/SOT SYNC status per lane.

8.2.2.13. CAL_ERROR_LANES

Offset: 0x18A
 Default: 0x00
 Description: Calibration error status per lane

Bit	Name	Access	Description
7:0	CAL_ERROR_LANES	Read Only	Calibration error status per lane.

8.2.2.14. HS_ERR_LANES

Offset: 0x18B
 Default: 0x00
 Description: HS Data transfer error status per lane

Bit	Name	Access	Description
7:0	HS_ERR_LANES	Read Only	HS Data transfer error status per lane.

8.2.2.15. HS_TEST_CNT

Offset: 0x18C
 Default: 0x00
 Description: Number of HS test received for lane N where N is controlled by HS_CNT_MUX

Bit	Name	Access	Description
31:0	HS_TEST_CNT	Read Only	Number of HS test received for lane N where N is controlled by HS_CNT_MUX.

8.2.2.16. LPDT_TEST_CNT

Offset: 0x190
Default: 0x00
Description: Number of LPDT test received

Bit	Name	Access	Description
31:0	LPDT_TEST_CNT	Read Only	Number of LPDT test received.

8.2.2.17. TRIGGER_TEST_CNT

Offset: 0x194
Default: 0x00
Description: Number of TRIGGER test received

Bit	Name	Access	Description
31:0	TRIGGER_TEST_CNT	Read Only	Number of TRIGGER test received.

8.2.2.18. ULPS_TEST_CNT

Offset: 0x198
Default: 0x00
Description: Number of ULPS test received

Bit	Name	Access	Description
31:0	ULPS_TEST_CNT	Read Only	Number of ULPS test received.

8.2.2.19. TG_RX_OVRD_DATA_PAT

Offset: 0x1A8
Default: 0x00
Description:

Bit	Name	Access	Description
31:24	TG_RX_OVRD_DATA_PAT_DATA_PAT_OVRD	Read Write	Data pattern override (1 bit per data lane).
23:16	TG_RX_OVRD_DATA_PAT_LP_DATA	Read Write	LP data pattern to use for checking instead of the generated pattern.
15:0	TG_RX_OVRD_DATA_PAT_HS_DATA	Read Write	HS data pattern to use for checking instead of the generated pattern. NOTE: checker will not be able to compute THS-SKIP if HS-DATA is all 0's or all 1's.

8.2.2.20. TG_RX_BIT_ERROR_CNT

Offset: 0x1B0

Default: 0x00

Description: Number of bit error found on lane N where N is controlled by HS_CNT_MUX

Bit	Name	Access	Description
63:0	TG_RX_BIT_ERROR_CNT	Read Only	Number of bit error found on lane N where N is controlled by HS_CNT_MUX.

8.2.2.21. TG_RX_HS_TXFER_CNT

Offset: 0x1B8

Default: 0x00

Description: HS RX total transfer count per lane (from any lane)

Bit	Name	Access	Description
63:0	TG_RX_HS_TXFER_CNT	Read Only	HS RX total transfer count per lane (from any lane).

8.2.2.22. TG_LINK_CONTROL

Offset: 0x1C0

Default: 0x00

Description:

Bit	Name	Access	Description
5:3	TG_LINK_CONTROL_HS_CNT_MUX	Read Write	Selects which lanes is read for some CSR registers.
2:0	TG_LINK_CONTROL_TEST_LANE_NUM	Read Write	Set number of lanes to test. If set higher than IP's lane numbers, it will test all lanes: 100 - 1 D-lane 101 - 2 D-lanes 110 - 4 D-lanes
<i>continued...</i>			

Bit	Name	Access	Description
			111 - 8 D-lanes 0XX - num lanes controlled through test_num pins.

8.2.2.23. TG_INIT_CNT

Offset: 0x1C4
Default: 0x400
Description: Number of ESC clock cycles for TX INIT

Bit	Name	Access	Description
31:0	TG_INIT_CNT	Read Write	Number of ESC clock cycles for TX INIT.

8.2.2.24. TG_HS_LEN

Offset: 0x1C8
Default: 0x00
Description:

Bit	Name	Access	Description
31	TG_HS_LEN_HS_LEN_OVRD_EN	Read Write	HS length override enable 1 - use register value as length 0 - hs len is generated by TG
30:0	TG_HS_LEN_HS_LEN	Read Write	HS transfer length in Uis (lower 3 bits are ignored - rounded down to # of bytes).

8.2.2.25. TG_LP_LEN

Offset: 0x1CC
Default: 0x400
Description:

Bit	Name	Access	Description
6:0	TG_LP_LEN_LP_LEN_OVRD_EN	Read Write	LPDT transfer length in bytes.

8.2.2.26. TG_SKEW_CAL

Offset: 0x1D0

Default: 0x20

Description: Initial skew calibration length in UI (rounded down to number of PPI access)

Bit	Name	Access	Description
31	TG_SKEW_CAL_INIT_SKEW_UNMASK	Read Write	Init skew calibration unmask enable 1 - enable init skew calibration generation after test restart 0 - disable init skew calibration generation after test restart Note: Under normal operation, init skew is only done on D-PHY link after device TINIT and D-PHY IP automatically does that. This bit enables driving init skew again for testing/debug.
30:0	TG_SKEW_CAL_INIT_SKEW_CAL_LEN	Read Write	Initial skew calibration transfer length in UIs (lower 3 bits are ignored - rounded down to # of bytes).

8.2.2.27. TG_ALT_CAL

Offset: 0x1D4

Default: 0x40

Description: Alternate skew calibration length in UI (rounded down to number of PPI access)

Bit	Name	Access	Description
31	TG_ALT_CAL_ALT_CAL_UNMASK	Read Write	Alternate calibration unmask enable 1 - enable alternate calibration generation after test restart 0 - disable alternate calibration generation after test restart Note: Under normal operation, alternate skew is only done on D-PHY link after the init calibration and D-PHY IP automatically does that. This bit enables driving alternate calibration again for testing/debug.
30:0	TG_ALT_CAL_ALT_CAL_LEN	Read Write	Alternate skew calibration transfer length in UIs (lower 3 bits are ignored - rounded down to # of bytes).

8.2.2.28. TG_PER_SKEW_CAL_LEN

Offset: 0x1D8

Default: 0x04

Description:

Bit	Name	Access	Description
31:0	TG_PER_SKEW_CAL_LEN	Read Write	

8.2.2.29. TG_TEST_CNT

Offset: 0x1E0
Default: 0x00
Description: Number of test round completed by TG

Bit	Name	Access	Description
31:0	TG_TEST_CNT	Read Only	Number of test round completed by TG.

8.2.2.30. TG_OVRD_DATA_PAT

Offset: 0x1E8
Default: 0x00
Description:

Bit	Name	Access	Description
31:24	TG_OVRD_DATA_PAT_DATA_PAT_OVRD	Read Write	Data pattern override (1 bit per data lane).
23:16	TG_OVRD_DATA_PAT_LP_DATA	Read Write	LP data pattern to TX instead of generated pattern.
15:0	TG_OVRD_DATA_PAT_HS_DATA	Read Write	HS data pattern to use instead of TG generated pattern. NOTE: checker will not be able to compute THS-SKIP if HS-DATA is all 0's or all 1's.

8.2.2.31. TG_TX_HS_TXFER_CNT

Offset: 0x1F0
Default: 0x00
Description: HS TX total transfer count per lane (on any lane)

Bit	Name	Access	Description
63:0	TG_TX_HS_TXFER_CNT	Read Only	HS TX total transfer count per lane (on any lane).



9. Verification Test Plan

The verification test plan for the MIPI D-PHY IP ensures that the MIPI D-PHY IP can achieve the required quality, functionality, and performance targets.

9.1. MIPI D-PHY Tests

The MIPI D-PHY IP is tested through both simulation and hardware verification. These tests are in accordance with the MIPI Alliance Conformance test suite, which includes the following:

- Data lane LP -TX signaling
- Clock lane LP -TX signaling
- Data lane HS -TX signaling
- Clock lane HS -TX signaling
- HS-TX clock to data lane timing
- TX init and ultra low power state
- LP -RX voltage and timing
- LP -RX behavioural
- HS -RX voltage and setup/hold
- HS -RX timer

Contact Altera for additional information related to compliance tests.

10. Document Revision History for the MIPI D-PHY IP User Guide

Document Version	Quartus Prime Version	IP Version	Changes
2025.03.30	25.1	5.0.0	<ul style="list-style-type: none"> Added support for Agilex 3 devices Added <i>Compiling the Altera MIPI D-PHY Design Example</i> Added <i>Simulating the IP</i> Added <i>Validating the IP</i> Added <i>Debugging the IP</i>
2025.01.13	24.3.1	4.0.0	<ul style="list-style-type: none"> In the <i>Introduction</i> chapter, made minor editorial changes to the <i>Introduction</i> topic. In the <i>Architecture</i> chapter, added a paragraph before the timing diagram. In the <i>Interface Design Guidelines</i> chapter, added content to the <i>I/O Bank Sharing</i> topic. In the <i>Configuring and Generating</i> chapter, modified the <i>Link Calibration Configuration</i> section in the <i>Configuring the MIPI D-PHY RX Mode</i> and <i>Configuring the MIPI D-PHY TX Mode</i> topics. Added the <i>Verification Test Plan</i> chapter.
2024.09.30	24.3	3.1.0	<ul style="list-style-type: none"> In the <i>Interface Design Guidelines</i> chapter: <ul style="list-style-type: none"> Removed the <i>MIPI Interface Layout Design Guidelines</i> topic from this chapter and added a note referring readers to the <i>High-Speed Signal Printed Circuit Board (PCB) Design Guidelines (HSSI, EMIF, MIPI, LVDS, PDN)</i> document. Removed the <i>Supported I/O Features in MIPI D-PHY I/O Standard</i> topic. Modified the table in the <i>Identifying Pin Assignments Based on Byte Location</i> topic. Modified the <i>Using the Remaining I/O Pin from Same Byte Location</i> topic.

			<ul style="list-style-type: none"> In the <i>Interface Signals and Register Maps</i> chapter: <ul style="list-style-type: none"> in the <i>D-PHY RX PPI Interface Signals</i> topic: <ul style="list-style-type: none"> Modified the <i>LINKn_CK_RxDataWidthHS</i> description in the <i>PPI RX Interface - Link n, Clock Lane</i> table, Modified the <i>LINKn_Dm_RxDataWidthHS</i> description in the <i>PPI RX Interface - Link n, Data Lane m</i> table, Modified the <i>LINKn_Dm_RxDataHS</i> description in the <i>PPI RX Interface - Link n, Data Lane m</i> table, Modified the <i>LINKn_Dm_RxValidHS</i> description in the <i>PPI RX Interface - Link n, Data Lane m</i> table. in the <i>D-PHY TX PPI Interface Signals</i> topic: <ul style="list-style-type: none"> Modified the <i>LINKn_CK_TxWordClkHS</i> description in the <i>PPI TX Interface - Link n, Clock Lane</i> table, Modified the <i>LINKn_CK_TxWordValidHS</i> description in the <i>PPI TX Interface - Link n, Clock Lane</i> table, Modified the <i>LINKn_Dm_TxWordClkHS</i> description in the <i>PPI TX Interface - Link n, Data Lane m</i> table, Modified the <i>LINKn_Dm_TxDataWidthHS</i> description in the <i>PPI TX Interface - Link n, Data Lane m</i> table, Modified the <i>LINKn_Dm_TxDataHS</i> description in the <i>PPI TX Interface - Link n, Data Lane m</i> table, Modified the <i>LINKn_Dm_TxWordValidHS</i> description in the <i>PPI TX Interface - Link n, Data Lane m</i> table, Modified the <i>Description</i> field in the <i>TX_CAP</i> topic.
2024.07.08	24.2	3.0.0	<ul style="list-style-type: none"> In the <i>Interface Design Guidelines</i> chapter: <ul style="list-style-type: none"> Added the <i>CLK</i> signal name to the <i>Identifying Pin Assignments Based on Byte Location</i> topic. Added <i>LVC MOS1.1</i> to the <i>Using the Remaining I/O Pin from Same Byte Location</i> topic.

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			<ul style="list-style-type: none"> • In the <i>Configuring and Generating</i> chapter: <ul style="list-style-type: none"> — Updated both figures in the <i>Configuring the D-PHY IP Tab</i> topic. — In the <i>Configuring the MIPI D-PHY RX Mode</i> topic: <ul style="list-style-type: none"> • Updated all three figures. • Added Rx Equalization mode parameter to the <i>Link Calibration Parameters</i> table. • Changed the default values for several parameters in the <i>Link RX Timing Configuration Parameters</i> table. — In the <i>Configuring the MIPI D-PHY TX Mode</i> topic: <ul style="list-style-type: none"> • Updated all three figures. • Added a sentence to the <i>Link Calibration Configuration</i> section. • In the <i>Link Calibration Parameters</i> table, changed the description and settings for the <i>Tx Equalization mode</i> parameter. • Changed the default values for several parameters in the <i>Link TX Timing Parameters</i> table. — In the <i>Simulating MIPI D-PHY IP Design Example with Modelsim* and Questasim*</i> topic, added a new step 7 to the procedure. • Changed several occurrences of Intel to Altera, throughout.
2024.04.01	24.1	2.2.0	Initial release.